



New Features in SMASH 5.14.0,
SCROOGE 2.3.0 & SHAKER 5.14.0

December 21, 2009

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THANKS

As always for new releases, we would like to thank those customers who take the time to report problems and/or to suggest improvements (please remember that the best way to do so is by sending an email to medal@dolphin-integration.com or support@dolphin-integration.com with an accurate description of your problem or suggestion, together with the relevant files if any). As you will see in the new features, we do our best to take remarks into account. And even if your suggestion does not appear this time, don't think it was lost or disregarded. Simply, it means that its implementation could not fit into the development plan for this particular release, but be assured that we will try to take it into account in a future release.

WEB SITE

Our web site <http://www.dolphin-integration.com> is a source of information on our EDA solutions. Aside from evaluation kits for our products, a number of application notes, courses or upgrades are available for download.

SMASH

The Application Hardware Modeling (AHM) approach consists in checking an overall function performed jointly by parts of the system, comprising some Virtual Component (so called ViC or silicon IP blocks) within a SoC assembled on the PCB with discrete components, such as Quartz, PMIC, or MEMS, along with application software. Assembling such Application Schematics (ASC) requires compliance with a variety of models at different description levels in order to perform complete multi-level, up to multi-domain, and mixed-signal design performance verifications.

SMASH 5.14 delivers major enhancements for designer productivity!

PSL

Relevant options of SMASH include native support for simulation of PSL (Property Specification Language) properties, both assertions and coverage, with very low time and memory overhead.

The integration of PSL is complete with source code syntax coloring, association of verification units with Verilog or VHDL models or instances, logging of PSL assertion violations, reporting of PSL sequence coverage results, and breaking into the source level debugger for investigation of design defects.

Assertion-Based Verification

The SLED ABV option enables conversion of PSL assertions into synthesizable RTL models. This makes it possible for the designer to automatically integrate PSL verification units into a Design Under Test in an FPGA for emulation or in a testchip. Embedding hardware verification units in prototypes increases verification speed by several orders of magnitude.

Automated generation of synthesizable models from PSL assertions can also be used as an efficient alternative to writing safety related parts of a design directly in RTL. These hardware verification units are integrated for embedded monitoring.

SUPPORTED PLATFORMS

Microsoft Windows

SMASH is designed to run under Microsoft Windows 2000/XP/Vista, both 32 bit and 64 bit platforms.

Sun Solaris on SPARC platform

SMASH is designed to run under Sun Solaris 7, 8 and 9 on the SPARC platform.

Linux on Intel x86 platform

SMASH is designed to run under the Linux distributions on the i86 platform detailed in the following table and depending on the embedded porting component.

SMASH is developed and validated mainly on RedHat Linux. However, customers deploy on various Linux distributions without any issues.

CREDITS & COPYRIGHTS

wxWidgets: A free C++ framework for cross-platform programming

<http://www.wxwidgets.org>

wxWindows Library License, Version 3

Copyright (C) 1998 Julian Smart, Robert Roebing [, ...]

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Scintilla Source Code Editor Component

License for Scintilla and SciTE

Copyright 1998-2005 by Neil Hodgson <neilh@scintilla.org>

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Trio: portable and extendable printf and string functions

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Gear-Brayton Integration Method

The new formulation of the Gear-Brayton integration method included in SMASH was perfected and implemented at Supélec - Service des Mesures.

EKV3 Compact MOSFET Model Documentation

A. Bazigos, M. Bucher, F. Krummenacher, J.-M. Sallese, A.-S. Roy, C. Enz, "*EKV3 Compact MOSFET Model Documentation, Model Version 301.01*", Technical Report, Technical University of Crete, November 23, 2007.

VDA / FAT Open Source Library

The open source library of VHDL-AMS components created by the VDA / FAT working group is delivered with SMASH.

The VDA / FAT Working Group AK 30 "Simulation of Mixed Systems with VHDL-AMS" is organized within the Association for Research in Automobile Technology (FAT - Forschungsvereinigung Automobiltechnik) of the German Association of the Automotive Industry (VDA - Verband der Automobilindustrie). It promotes the relationship between car manufactures and their suppliers concerning simulation of mixed systems and model exchange.

The working group promotes the development of VHDL-AMS models that are integrated in different libraries.

FUNDAMENTALS_VDA

Public library with general VHDL-AMS models like time sources, converters between different domains, table-lookup models, relays, switches...

SPICE2VHD

VHDL-AMS models with nearly the same terminal behavior like Spice models of basic electrical elements like resistor, capacitor, inductor, and level1 models of semiconductor devices.

AUTOMOTIVE_VDA

Library under development with special parameterized models like wires, fuses, bulbs, EMC test signals...

SMASH - Viewer

Enhancements

- Implemented display of Verilog variables in transient windows and reloaded in generic waveform windows (DDIsa01066 - SMASH 5.14.0).
- Improved behavior of formula dialog to show the traces tab by default and to not close after plotting a formula (DDIsa04372 - SMASH 5.14.0).
- Implemented text editor source code folding for SPICE netlists (DDIsa05268 - SMASH 5.14.0).
- Implemented using analog waveforms of logic signals in the formula creation dialog (DDIsa05427 - SMASH 5.14.0).

Modifications

- Modified Unix launcher scripts to allow spaces in arguments (DDIsa05440 - SMASH 5.14.0).
- Modified display of shared library revision numbers in report file to only display revision numbers relevant for loaded circuit (DDIsa05447 - SMASH 5.14.0).

Bug fixing

- Corrected handling of the Preferences dialog that caused the licensing configuration to be changed when clicking the OK button without opening the licensing pane (SMASH 5.14.0).
- Corrected an infinite loop which occurred when performing a text search for a no longer existing string or when at the end of the file (DDIsa05365 – SMASH 5.14.0).
- Corrected crash that occurred when saving waveform traces if the simulator control file was not open (DDIsa05378 - SMASH 5.14.0).
- Corrected dependency handling so that circuit is not reloaded after saving waveform window traces (DDIsa05379 - SMASH 5.14.0).
- Corrected handling of the "Save intermediate files..." setting in the Imbalance Locate dialog box (DDIsa05380 - SMASH 5.14.0).
- Corrected regression in logic waveform display at the end of the simulation which was incomplete (DDIsa05402 - SMASH 5.14.0).
- Corrected missing file close for waveform files after reloading waveforms during Monte Carlo runs (DDIsa05438 - SMASH 5.14.0).
- Corrected initialization of the periodic logic event used to display the progress-bar during simulation which could cause a simulation slowdown (DDIsa05444 - SMASH 5.14.0).
- Corrected a crash that occurred when hitting the help button in a dialog (DDIsa05470 - SMASH 5.14.0).
- Corrected a Tcl stack overflow that could occur in the script handling the display of the Files view pane (DDIsa05483 - SMASH 5.14.0).

- Corrected handling of side by side display of nsx/pat so that netlist file (.nsx) is not displayed when the simulator control file is not a pattern file (.pat) (DDIsa05486 - SMASH 5.14.0).
- Modified shared library linking to avoid a crash that could occur after a network disconnection when using compiled models on remote disk (DDIsa05487 - SMASH 5.14.0).

SCROOGE - Viewer

Enhancements

- Implemented access to previous power reports from the Files panel after circuit load (DDIsa05332 - SCROOGE 2.3.0).

Bug fixing

- Corrected AQD(t) plugin where setting and getting time values was not possible under Unix (DDIsa05099 - SCROOGE 2.3.0).
- Corrected crash caused by the icon animation that could occur when quitting SCROOGE (DDIsa05489 - SCROOGE 2.3.0).

SMASH - Batch

Modifications

- Modified Unix launcher scripts to allow spaces in arguments (DDIsa05440 - SMASH 5.14.0).

SMASH - Kernel

Enhancements

- Implemented display of Verilog variables in transient windows and reloaded in generic waveform windows (DDIsa01066 - SMASH 5.14.0).
- Implemented .FFT directive allowing to automatically launch an FFT analysis after a transient analysis (DDIsa01117 - SMASH 5.14.0).
- Implemented order independent elaboration of .PARAM statements when parsing and loading circuit description (DDIsa02105 - SMASH 5.14.0).
- Optimized matrix linking to accelerate analog circuit elaboration and composed analyses such as Monte Carlo (DDIsa02233 - SMASH 5.14.0).
- Implemented .FFT directive allowing to automatically launch an FFT analysis for each run of a sweep analysis (DDIsa02252 - SMASH 5.14.0).
- Implemented possibility to use library file parameters in the simulator control file (DDIsa02269 - SMASH 5.14.0).

- Improved SPICE parsing so that sub-circuit local parameters can be specified as sub-circuit instance parameters (DDIsa03119 - SMASH 5.14.0).
- Implemented .FFT directive allowing to launch FFT analysis and to save FFT waveform files (DDIsa05490 - SMASH 5.14.0).

Modifications

- Improved reporting when simulation is stopped due to VHDL assert statement with severity "failure" (DDIsa05331 - SMASH 5.14.0).
- Completed detection of multiple instantiations from SPICE testbenches of logic instances with the same hierarchical name (DDIsa05382 - SMASH 5.14.0).
- Optimized implementation of HiCUM v2.23 bipolar model to increase simulation speed (DDIsa05390 - SMASH 5.14.0).
- Modified waveform file handling to only create the BWF file if it will contain some waveforms (DDIsa05437 - SMASH 5.14.0).
- Modified display of shared library revision numbers in report file to only display revision numbers relevant for loaded circuit (DDIsa05447 - SMASH 5.14.0).
- Modified instantiation of .VEC directives in order to allow more than one (DDIsa05508 - SMASH 5.14.0).

Bug fixing

- Corrected handling of simulation log file for Monte Carlo and Sweep analyses which were issuing an error message (DDIsa04550 - SMASH 5.14.0).
- Corrected a crash that occurred when searching for HiZ nets in a Verilog-A module (DDIsa05386 - SMASH 5.14.0).
- Corrected calculation of operating-point using homotopy method which could crash in presence of ABCD blocks in the circuit (DDIsa05388 - SMASH 5.14.0).
- Corrected handling of operating-point stepping method when it fails before reaching the final GMIN value (DDIsa05399 - SMASH 5.14.0).
- Corrected missing interface device insertion when instantiating a SPICE model from Verilog with a connection expression (DDIsa05413 - SMASH 5.14.0).
- Corrected SPICE sub-circuit instantiation from Verilog using "named port" style which was using port order instead of port name (DDIsa05415 - SMASH 5.14.0).
- Corrected transient noise simulation when swift mode is active which was slowed sufficiently to be unusable (DDIsa05441 - SMASH 5.14.0).
- Corrected a crash that occurred when starting an analysis with Laplace devices and the .PRINTALL directive (DDIsa05477 - SMASH 5.14.0).

- Modified shared library linking to avoid a crash that could occur after a network disconnection when using compiled models on remote disk (DDIsa05487 - SMASH 5.14.0).
- Corrected handling of tolerances when using .OPTION EPS which could cause a crash under certain conditions (DDIsa05491 - SMASH 5.14.0).
- Corrected handling of SDF file so that it is closed when the annotation fails (DDIsa05492 - SMASH 5.14.0).
- Corrected initialization of configuration values from defaults.ini which were not read at the first run when in co-simulation mode (DDIsa05514 - SMASH 5.14.0).
- Corrected the extraction of the right bound value of logic vector port ranges which was limited to 256 (DDIsa05519 - SMASH 5.14.0).

SMASH - SPICE

Enhancements

- Implemented .FFT directive allowing to automatically launch an FFT analysis after a transient analysis (DDIsa01117 - SMASH 5.14.0).
- Implemented order independent elaboration of .PARAM statements when parsing and loading circuit description (DDIsa02105 - SMASH 5.14.0).
- Optimized matrix linking to accelerate analog circuit elaboration and composed analyses such as Monte Carlo (DDIsa02233 - SMASH 5.14.0).
- Implemented .FFT directive allowing to automatically launch an FFT analysis for each run of a sweep analysis (DDIsa02252 - SMASH 5.14.0).
- Implemented possibility to use library file parameters in the simulator control file (DDIsa02269 - SMASH 5.14.0).
- Improved SPICE parsing so that sub-circuit local parameters can be specified as sub-circuit instance parameters (DDIsa03119 - SMASH 5.14.0).
- Implemented the foundation for providing file name and line number information in SPICE parsing errors and warnings (DDIsa03760 - SMASH 5.14.0).
- Implemented instantiation of SPICE primitives from Verilog-AMS (DDIsa05001 - SMASH 5.14.0).
- Updated BSIM3 and BSIM4 model ACM calculations (ad, as, pd, ps) for compatibility with HSpice model parameter sets using GEOSHRINK (DDIsa05417 - SMASH 5.14.0).
- Implemented .FFT directive allowing to launch FFT analysis and to save FFT waveform files (DDIsa05490 - SMASH 5.14.0).

Bug fixing

- Corrected calculation of operating-point using homotopy method which could crash in presence of ABCD blocks in the circuit (DDIsa05388 – SMASH 5.14.0).
- Corrected handling of operating-point stepping method when it fails before reaching the final GMIN value (DDIsa05399 - SMASH 5.14.0).
- Corrected missing interface device insertion when instantiating a SPICE model from Verilog with a connection expression (DDIsa05413 - SMASH 5.14.0).
- Corrected SPICE sub-circuit instantiation from Verilog using "named port" style which was using port order instead of port name (DDIsa05415 - SMASH 5.14.0).
- Corrected a crash that occurred when starting an analysis with Laplace devices and the .PRINTALL directive (DDIsa05477 - SMASH 5.14.0).
- Corrected handling of tolerances when using .OPTION EPS which could cause a crash under certain conditions (DDIsa05491 - SMASH 5.14.0).

SMASH - Verilog & Verilog-AMS

Enhancements

- Implemented display of Verilog variables in transient windows and reloaded in generic waveform windows (DDIsa01066 - SMASH 5.14.0).
- Implemented instantiation of SPICE primitives from Verilog-AMS (DDIsa05001 - SMASH 5.14.0).
- Implemented support of Laplace operator in Verilog-A (DDIsa05315 - SMASH 5.14.0).

Modifications

- Completed detection of multiple instantiations from SPICE testbenches of logic instances with the same hierarchical name (DDIsa05382 - SMASH 5.14.0).
- Improved behavior of transition, slew and delay operators in Verilog-A (DDIsa05349 - SMASH 5.14.0).

Bug fixing

- Corrected detection of vectors in expressions and assignments when generating optimized Verilog models (DDIsa05343 - SMASH 5.14.0).
- Corrected saving in VCD files of big logic vectors which were not saved correctly due to an insufficient buffer size (DDIsa05351 - SMASH 5.14.0).
- Corrected a crash that occurred when searching for HiZ nets in a Verilog-A module (DDIsa05386 - SMASH 5.14.0).
- Corrected missing interface device insertion when instantiating a SPICE model from Verilog with a connection expression (DDIsa05413 - SMASH 5.14.0).

- Corrected SPICE sub-circuit instantiation from Verilog using "named port" style which was using port order instead of port name (DDIsa05415 - SMASH 5.14.0).
- Corrected the extraction of the right bound value of logic vector port ranges which was limited to 256 (DDIsa05519 – SMASH 5.14.0).

SMASH - VHDL & VHDL-AMS

Modifications

- Improved reporting when simulation is stopped due to VHDL assert statement with severity "failure" (DDIsa05331 - SMASH 5.14.0).

Bug fixing

- Corrected VHDL code generation name collision when hierarchical blocks with same name declare signals with identical names (DDIsa04492 - SMASH 5.14.0).
- Corrected saving in VCD files of big logic vectors which were not saved correctly due to an insufficient buffer size (DDIsa05351 - SMASH 5.14.0).
- Corrected VHDL/VHDL-AMS intermediate format revision number to avoid a crash when loading a circuit compiled with SMASH 5.13.0 (DDIsa05446 - SMASH 5.14.0).
- Corrected the extraction of the right bound value of logic vector port ranges which was limited to 256 (DDIsa05519 – SMASH 5.14.0).

SMASH - PSL

Enhancements

- Implemented support for SERE operators in PSL properties (DDIsa05171 - SMASH 5.14.0).
- Implemented generation of synthesizable detectors from PSL properties (DDIsa05173 - SMASH 5.14.0).

SMASH - Models (C, D, E, F, G, H, I, J, K, L, M, Q, R, T, U, V)

Enhancements

- Updated BSIM3 and BSIM4 model ACM calculations (ad, as, pd, ps) for compatibility with HSpice model parameter sets using GEOSHRINK (DDIsa05417- SMASH 5.14.0).

Modifications

- Optimized implementation of HiCUM v2.23 bipolar model to increase simulation speed (DDIsa05390 - SMASH 5.14.0).

Bug fixing

- Corrected transient noise simulation when swift mode is active which was slowed sufficiently to be unusable (DDIsa05441 – SMASH 5.14.0).
- Corrected a crash that occurred when starting an analysis with Laplace devices and the .PRINTALL directive (DDIsa05477 – SMASH 5.13.2).

SMASH - SDF

Bug fixing

- Corrected handling of SDF file so that it is closed when the annotation fails (DDIsa05492 - SMASH 5.14.0).

SMASH - API, Extensions & Plug-ins

Bug fixing

- Corrected initialization of configuration values from defaults.ini which were not read at the first run when in co-simulation mode (DDIsa05514 – SMASH 5.14.0).

SMASH - Licensing

Enhancements

- Improved licensing configuration storage to simplify license setup for multiple Dolphin applications and share it with SLED (DDIsa05500 - SMASH 5.14.0).

Bug fixing

- Corrected handling of the Preferences dialog that caused the licensing configuration to be changed when clicking the OK button without opening the licensing pane (SMASH 5.14.0).

SHAKER

Modifications

- Implemented means for SHAKER to run a specific analysis for bisection with SMASH using a custom Tcl script (DDIsa03470 - SMASH 5.14.0).

Bug fixing

- Corrected SHAKER configuration file so that the measure files generated by SMASH are loaded (DDIsa05420 - SHAKER 5.14.0).