

Switched-Current Circuit Design and Simulation

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Gerson Machado⁺ and Cyril Descleves⁺⁺

⁺Department of Electrical and Electronic Engineering
Imperial College, London SW7 2BT England

⁺⁺Dolphin Integration, B.P 65 ZIRST
38242 Meylan Cedex France

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INTRODUCTION

Competition in the area of mixed analog and digital MOS ICs has been pushing analog designers towards using pure digital VLSI/ULSI processes for both the analog and digital parts of the IC. Generally, the analog part of a mixed-mode IC takes longer to design but occupies only a small percentage of the chip's area. This trend not only calls for new analog design techniques fully compatible with pure digital VLSI processes [1] but also it reveals limitations in the use of purely analog, purely digital, or circuit-level-only simulators as design tools.

This is particularly the case with current-mode analog sampled-data circuits (or switched-current - SI circuits), renowned for being one of the toughest kind of circuits to simulate [2]. They demand robust convergence algorithms coupled with realistic and continuous MOS models that will give meaningful results with reasonable simulation time, especially when fine-tuning circuit-level building blocks. For the fast and effective simulation of complete systems, it is necessary to use higher-level true-behavioral descriptions, formulated in a standard, non-proprietary language such as C; also desirable is an interface for standard HDLs. In its electrical and structural levels, SMASHTM can handle analog components as differential equations and digital components as Boolean laws and event-driven. At a behavioral level, circuit blocks can be substituted by either their Laplace-transform block or by a C-code model, ensuring quick system-level simulations.

The use of the mixed-mode multi-level simulation engine of the industry-proven SMASHTM simulator is illustrated with the switched-current (SI) technique. We show how the use of options, models and simulation hierarchy can affect the simulation of SI circuits and how SMASHTM can be used to obtain flexibility and speed in the design phase. The robust algorithms in SMASHTM, the availability of realistic MOS models and real-time graphics processing are shown to allow simulation and visualization of the toughest SI designs in any region of operation of MOS transistors. At circuit-level SMASHTM accounts for non-ideal device characteristics and at system-level it combines descriptions of SI cells to avoid excessive simulation time. SMASHTM can easily handle typical mixed-mode systems such as PLLs [3] or sigma-delta data converters (analog modulator and digital filtering).

The first part of this application note deals with an example of a saturated, regulated-cascode SI memory cell. In the second part we use SMASHTM to simulate a new class of SI circuits using the S²I technique, for transistors biased in the transition of weak to moderate regions. In a third part we discuss the simulation of SI circuits at higher level to demonstrate the potential speed-advantage of higher level modeling.

1 - BACKGROUND

a) The EKV MOS Model Formulation and Usage

The very nature of analog-sampled-data systems based on techniques such as switched capacitors or switched currents mean that transient simulations are longer due to settling effects at each clock period. Increased simulation runs are expected in these systems due to intrinsic time discontinuities in the signal processing strategy. This problem can be compounded if MOS models are discontinuous and non-realistic themselves, particularly between regions of transistor operation (weak, moderate, strong inversion). This would not only cause increased convergence problems and simulation time but would also lead to false results with respect to stored charges and node voltages. In SMASHTM the user has a choice beyond the traditional SPICE models found in other simulators. SMASHTM allows you to choose between two industry-proven continuous and precise MOS models (the EKV model from École Polytechnique Fédérale de Lausanne - EPFL or the AMS model from Austria Micro Systems) or to implement your own model in C code without having to resort to proprietary modeling languages. Moreover, the extra MOS models in SMASHTM use a relatively small number of parameters which are not only easily obtainable [4] but also will give the user a computational advantage for statistical simulations compared to other simulators with non-intuitive proprietary models and hard-to-find parameters.

In this application note we use the EKV model from EPFL throughout [5,6]. A detailed description of the EKV model formulation and usage is to be found elsewhere [6,7] but for convenience equations of interest are presented here. The intrinsic symmetry of the device is preserved by referring V_G , V_D and V_S to the local substrate. The drain current I_D is expressed as $I_D = I_F - I_R$ where $I_F(V_G, V_S)$ is the forward component of the current (independent of V_D) and $I_R(V_G, V_D)$ is the reverse component of the current (independent of V_S):

$$I_{F(R)} = I_S \cdot \ln^2 \left(1 + e^{\left(\frac{V_G - V_{TO} - nV_{S(D)}}{2nU_T} \right)} \right) \text{ with the thermodynamic voltage } U_T = k \cdot T / q \text{ (26mV at 300K), the specific current}$$

$I_S = 2 \cdot n \cdot \beta \cdot U_T^2$, and the transfer parameter $\beta = \mu \cdot C_{ox} \cdot W_{eff} / L_{eff}$). The slope factor n is usually smaller than 2 and tends to 1 for very large values of V_G . It can be estimated in weak inversion from the $\log I_D \times V_G$ curve by $slope = S = 1/n \cdot U_T$ (in SPICE 2,3 the absolute values of I_D are wrong but the slopes can be correct if foundries properly characterize the parameter NFS). When S in mV/decade of I_D is supplied, n can be directly calculated from $n \approx 5.04 (S/T)$ where T is the temperature in Kelvin. SMASHTM will provide the user with the value of $n(V_G)$ after an operating point analysis when you use the option BIASINFO=LONG MODELINFO=LONG. In table I the current $I_D = I_F - I_R$ is expressed for a number of modes of operation of the MOST [6,7] except bipolar. If $I_{F(R)} \ll I_S$ (or $V_G < V_{TO} + nV_{S(D)}$) this component is in weak inversion-WI. If $I_{F(R)} \gg I_S$ (or $V_G > V_{TO} + nV_{S(D)}$) this component is in strong inversion-SI. The transistor is said to be in conduction when both I_F and I_R are in SI. If only one I_D component is in SI then the other is negligible and the transistor is in saturation (forward and independent of V_D or reverse and independent of V_S).

In analog design, operation in the moderate inversion region of the MOST is frequently required. In the current version of the EKV model explicit expressions valid in all regions are formulated through the definition of a transconductance interpolation function $G(i)$ between WI and SI regions. Forward and reverse normalized currents are defined as $i_f = I_F / I_S$ and $i_r = I_R / I_S$ (i_f is also called inversion factor or inversion coefficient IC for forward modes: $IC \gg 1$ in SI and $IC \ll 1$ in WI):

$$i_{f(r)} = e^{\frac{V_P - V_{S(D)}}{U_T}} = e^{\frac{V_G - V_{TO} - nV_{S(D)}}{nU_T}} \text{ in WI} \quad i_{f(r)} = \left(\frac{V_P - V_{S(D)}}{2U_T} \right)^2 = \left(\frac{V_G - V_{TO} - nV_{S(D)}}{2nU_T} \right)^2 \text{ in SI}$$

Tables II and III present respectively the small signal transconductances and the intrinsic capacitances in SI and WI. The transconductances in saturation are normalized to their maximum value reached in WI (table IV) using the interpolation function $G(i) \equiv \left(i + \frac{1}{2} \sqrt{i} + 1 \right)^{-1/2}$. Table V presents the intrinsic capacitances model.

Table I - Current I_D in SI and WI [6,7]

Conduction $I_D =$	<p style="text-align: center;">Weak Inversion</p> $2.n.\beta.U_T^2.e^{\frac{V_G-V_{T0}}{nU_T}} \left(e^{\frac{-V_S}{U_T}} - e^{\frac{-V_D}{U_T}} \right) \text{ for } \begin{cases} V_S > V_P = \frac{V_G-V_{T0}}{n} \\ \text{and} \\ V_D > V_P = \frac{V_G-V_{T0}}{n} \text{ or } I_{D0}.e^{\frac{V_G}{nU_T}} \left(e^{\frac{-V_S}{U_T}} - e^{\frac{-V_D}{U_T}} \right) \text{ with } I_{D0} = 2.n.\beta.U_T^2.e^{\frac{-V_{T0}}{nU_T}} \\ V_S \equiv V_D \end{cases}$
	<p style="text-align: center;">Strong Inversion</p> $n.\beta.(V_D - V_S) \left(V_P + \frac{V_S + V_D}{2} \right) \text{ for } \begin{cases} V_D < V_P = \frac{V_G-V_{T0}}{n} \\ \text{and} \\ V_S < V_P = \frac{V_G-V_{T0}}{n} \end{cases} \text{ or } \beta.(V_D - V_S) \left[V_G - V_{T0} - \frac{n}{2}.(V_D + V_S) \right]$
Forward (Reverse) Saturation $ I_D =$	<p style="text-align: center;">Weak Inversion</p> $I_S.e^{\frac{V_G-V_{T0}-nV_{S(D)}}{nU_T}} \text{ with } I_S = 2.n.\beta.U_T^2 \text{ or } I_{D0}.e^{\frac{V_G-nV_S}{nU_T}} \text{ for } \begin{cases} V_S > V_P \\ V_D > V_P \\ V_{DS} \gg U_T \end{cases}$
	<p style="text-align: center;">Strong Inversion</p> $\frac{n.\beta}{2} (V_P - V_{S(D)})^2 \text{ for } \begin{cases} V_S < V_P < V_D \text{ (if } I_D = I_F) \\ V_D < V_P < V_S \text{ (if } I_D = -I_R) \end{cases} \text{ or } \frac{\beta}{2n} (V_G - V_{T0} - nV_{S(D)})^2 \text{ or } \frac{I_S}{4} \left(\frac{V_P - V_{S(D)}}{U_T} \right)^2$
Blocked $I_D =$	<p style="text-align: center;">Weak Inversion</p> $I_F = I_R \Rightarrow I_D = 0 \text{ for } \begin{cases} V_S \gg V_P \\ \text{and} \\ V_D \gg V_P \end{cases} \text{ or } V_S = V_D$
	<p style="text-align: center;">Strong Inversion</p> $I_F = I_R \Rightarrow I_D = 0 \text{ for } \begin{cases} V_S > V_P \\ \text{and} \\ V_D > V_P \end{cases}$

Table II - Transconductances in SI and WI [6,7]

	Strong Inversion		WI
	Conduction	Forward Saturation	
g_{mg}	$\beta.(V_D - V_S)$	$\beta.(V_P - V_S) = \sqrt{\frac{2\beta.I_F}{n}} = \frac{2.I_F}{n.(V_P - V_S)} = \frac{I_F}{n.U_T.\sqrt{i_f}}$	$\frac{I_D}{n.U_T}$
g_{ms}	$n\beta.(V_P - V_S) = \sqrt{2n\beta}$	$n\beta.(V_P - V_S) = \sqrt{2n\beta.I_F} = \frac{2.I_F}{(V_P - V_S)} = \frac{I_F}{U_T.\sqrt{i_f}}$	$\frac{I_F}{U_T}$
g_{md}	$n\beta.(V_P - V_D) = \sqrt{2n\beta}$	≈ 0	$\frac{I_R}{U_T}$

Table III - Intrinsic Capacitances in SI and WI [6]

Normalized C	Strong Inversion		WI
	Conduction	Fwd & Rev Saturation	
C_{gs}/C_{ox}	$\frac{2}{3} \left[1 - \frac{i_r}{(\sqrt{i_f} + \sqrt{i_r})^2} \right]$	$\frac{2}{3}$	i_f
C_{gd}/C_{ox}	$\frac{2}{3} \left[1 - \frac{i_f}{(\sqrt{i_f} + \sqrt{i_r})^2} \right]$	≈ 0	i_r
C_{bs}/C_{ox}	$(n-1). \frac{C_{gs}}{C_{ox}}$		
C_{bd}/C_{ox}	$(n-1). \frac{C_{gd}}{C_{ox}}$		
C_{gb}/C_{ox}	$\frac{n-1}{3n} \left[1 - \frac{4.\sqrt{i_f}.i_r}{(\sqrt{i_f} + \sqrt{i_r})^2} \right]$	$\frac{n-1}{3.n}$	$1 - \frac{1}{n}$

Table IV - Transconductances interpolation [6]

g_{mg}	$2 \cdot \beta \cdot U_T (i_f \cdot G(i_f) - i_r \cdot G(i_r)) = \frac{I_F \cdot G(i_f)}{n \cdot U_T} - \frac{I_R \cdot G(i_r)}{n \cdot U_T}$
g_{ms}	$2 \cdot n \cdot \beta \cdot U_T \cdot i_f \cdot G(i_f) = \frac{I_F \cdot G(i_f)}{U_T}$
g_{md}	$2 \cdot n \cdot \beta \cdot U_T \cdot i_r \cdot G(i_r) = \frac{I_R \cdot G(i_r)}{U_T}$

Table V - Intrinsic capacitances for interpolation [6]

$\frac{C_{gs}}{C_{ox}}$	$\left(\frac{1}{c_{gss}(i_f, i_r)} + \frac{1}{c_{gsw}(i_f)} \right)^{-1}$
$\frac{C_{gd}}{C_{ox}}$	$\left(\frac{1}{c_{gss}(i_r, i_f)} + \frac{1}{c_{gsw}(i_r)} \right)^{-1}$
$\frac{C_{gb}}{C_{ox}}$	$\left(\frac{n-1}{n} \right) \cdot \left(1 - \frac{c_{gbs}(i_f, i_r) \cdot c_{gbw}(i_f, i_r)}{c_{gbs}(i_f, i_r) + c_{gbw}(i_f, i_r)} \right)$
where	
$c_{gss}(i_f, i_r) \equiv \frac{2}{3} \cdot \left[1 - \frac{i_r}{(\sqrt{i_f} + \sqrt{i_r})^2} \right]$; $c_{gss}(i_r, i_f) \equiv \frac{2}{3} \cdot \left[1 - \frac{i_f}{(\sqrt{i_f} + \sqrt{i_r})^2} \right]$	
$c_{gsw}(i_f) \equiv i_f \cdot G(i_f)$; $c_{gsw}(i_r) \equiv i_r \cdot G(i_r)$; $c_{gsw}(i_f, i_r) \equiv i_f \cdot G(i_f) + i_r \cdot G(i_r)$	
$c_{gbs}(i_f, i_r) \equiv \frac{2}{3} \cdot \left[1 + 2 \cdot \frac{\sqrt{i_f \cdot i_r}}{(\sqrt{i_f} + \sqrt{i_r})^2} \right]$	

b) The Switched Current Memory Cell Principle

The basic principle of a regulated cascode memory cell is discussed here. The reader is referred to [1] for further reading on the SI technique. The basic regulated cascode cell is shown below in figure 1 and comprises three transistors M1 M7 M5 which implement a half-delay $Z^{-1/2}$ to the input current. By cascoding two cells a full Z^{-1} delay is obtained. The cell operates as follows: during ϕ_1 , command ph1, M1 is diode-connected and its gate capacitance charges up until V_{GS1} is enough to maintain the drain current. The gate of M5 which is connected to the drain of M1 senses its V_{DS1} . Since M5 is biased with a constant current I_b , any difference between V_{DS1} and V_{GS5} is detected and amplified by the loop formed by M7 and M5 with a typical gain of 10.000. Thus V_{DS1} is maintained constant at V_{GS5} . During ϕ_2 , command ph2, M1 maintains the sampled drain current and the effect of any output variations on V_{DS1} gets reduced by the loop gain. The simulation is described in section 3, with the SMASHTM input files and the output curves.

The technique can be used for implementing integrators, differentiators, current multipliers and all conventional sampled-data signal processing blocks.

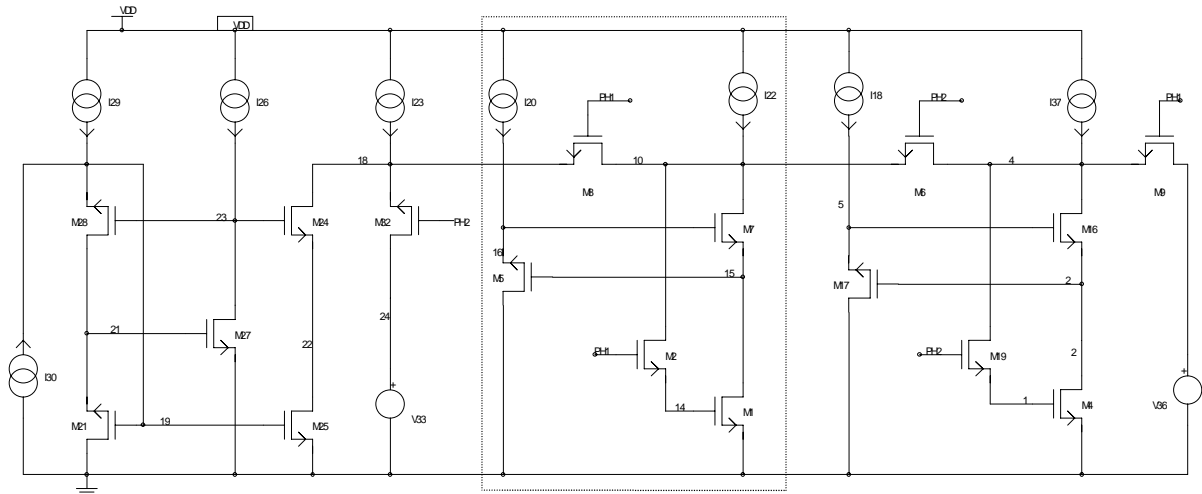


Figure 1: Regulated cascode SI delay element.

In order to overcome a number of limitations from the basic or enhanced SI cell the S^2I technique has been recently proposed [8]. More recently the S^2I class AB cell has been proposed as an alternative for low-power signal processing [9]. We will discuss this cell in this application note. The basic S^2I class AB circuit is shown in figure 2. In practice the cell can be cascoded to improve errors due to non-zero output conductance, particularly if the memory transistor is short. In our S^2I example, because we use the cell at very low current levels, timing of the controlling clocks is critical and rather than fully non-overlapping clocks optimum overlap is necessary for improved performance. In SMASH™ the best clocking scheme trade-off can be visualized quickly by using the .PARAM (parameter) feature as illustrated in the S^2I example. The critical nodes - gates of memory transistors - are switched slightly earlier than their respective drains to avoid storing errors due to switching. The operation of the circuit is similar to the simple S^2I cell [8] and is as follows. During $\Phi 1a$ the active memory cell samples the input current $i_{in}(n)$. During $\Phi 1b$ the stored current ($-i_{in} + \delta a$) of the active memory cell is subtracted from the input current leaving just the $-\delta a$ residual error which will be sampled by the 2nd memory cell. During $\Phi 2$ the current coming from the 2nd memory cell is $\delta b - \delta a$ that adds to the output of the first cell forming the overall output $i_{out} = -i_{in}(n) + \delta a + \delta b - \delta a = -i_{in}(n) + \delta b$. The error term δb can in theory become a δn term if we extend the number of fine-memory cells to n . However this complicates the clocking and takes more area, particularly for weakly-inverted transistors. The S^2I cancellation scheme allows the implementation of class AB SI cells with better performance than previously reported [1]. An example is shown in section 4 [9], based on the following schematics.

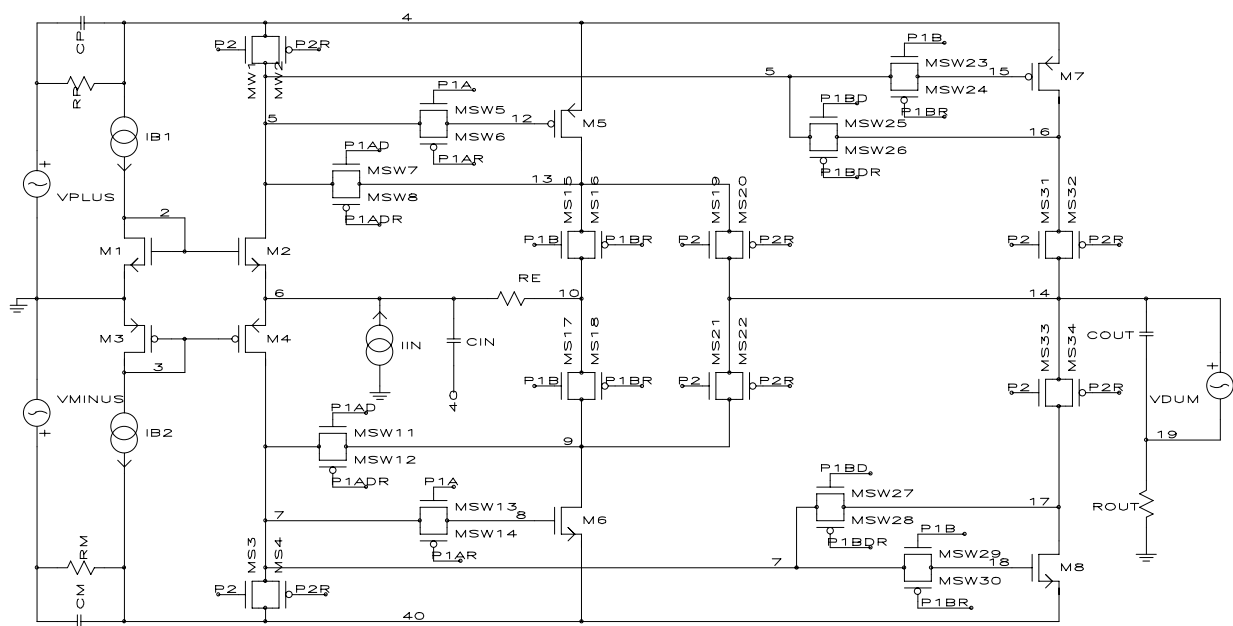


Figure 2: S^2I class AB cell

2 - Tips on selecting simulator parameters for a discrete-time simulation

Some tips for the straightforward simulation of analog sampled-data systems and in particular SI circuits using SMASHTM may be useful. If we define the speed in Hz of an SI cell as given by its g_{mg}/C_{in} ratio for a given bias current I_{bias} and we, say, allow 7 to 8 time constants for settling for equal-length input and output phases, then we can estimate around 16 time-constants τ needed within one sample-period T . If we clock our system at ten times the frequency equivalent to the sample-period T we can use $T/10$ as the period in our .PULSE voltage sources. In the .TRAN request a good rule of thumb is to ask for about 1000 points per each period T that we are simulating. Say we want to simulate 2 periods T (if we were performing a Fourier analysis to look at distortion we should have as many periods as possible to avoid numerical errors but to visualize the behavior of a circuit just one period would be OK). For the sake of this example let's say that $T=0.5\mu s$. Then we could have .TRAN 500E-12 1E-6, which corresponds to .TRAN (Tx2/2000) (Tx2) where one would note that 500E-12 should be around 10 times smaller than the smallest time-constant in our circuit.

A few words are due regarding the use of SMASHTM options for good precision and convergence with SI circuits (please refer to the convergence topics in the SMASHTM documentation). The first thing to check before starting a simulation are the parameters supplied to the simulator and the adequacy of the model you are using with the kind of circuit you are simulating. A good start is to always use the better continuous models like either EKV or AMS over the standard SPICE ones. A method to adapt SPICE 2,3 parameters to the EKV model in SMASHTM is described in [4]. The second thing to check is the topology and connectivity of your circuit. The most important simulation directives in SI circuits are the .EPS and .H directives which control respectively .TRAN & .POWERUP accuracy and the time-step control. Asking for too much .EPS precision may just make things difficult to converge or extremely time consuming. However if you're simulating at very low current levels you may have to put-up with the extra time to get meaningful results. It is always helpful to have in the .OP directive DELTAV set to a low value of say 100mV if you are dealing with subthreshold circuits and also to have BIASINFO=LONG and MODELINFO=YES. Also, both VMAX and VMIN should be set to compatible limits with respect to your power-supply, like around 10 to 15% above and below respectively. If a circuit does not converge within a reasonably requested precision you may need to increase the number of interactions MAXITER. In general the options used in the two application examples here will account for the vast majority of SI circuits. In the SMASHTM documentation however you can find out about other unique options in case of non-convergence but we will not deal with them here since their use has not been necessary.

3 - Example 1 - Regulated Cascode Memory Cell (saturated)

Figure 1 shows a regulated cascode memory cell operating in its saturation mode, not optimized. Design techniques for the circuit can be found in [1] and are not discussed here. Input files for SMASHTM corresponding to figure 1, are displayed below with necessary comments.

As soon as the simulation is started you can visualize the behavior of the circuit on-line, scale, add or delete graphs and decide whether to proceed or not. The simulation can also be interrupted and continued at a later time.

```

*-----file SIab.nsx-----
*Regulated cascode memory cell
*-----

M4 2 1 0 0 mn L=12 W=80
M19 4 3 1 0 mn L=2 W=16
M17 0 2 5 0 mn L=4 W=75
M9 7 6 4 0 mn L=2 W=8
M16 4 5 2 0 mn L=4 W=75
M6 4 8 10 0 mn L=2 W=8
M1 15 14 0 0 mn L=12 W=80
M2 10 6 14 0 mn L=2 W=16
M5 0 15 16 0 mn L=4 W=75
M7 10 16 15 0 mn L=4 W=75
M8 10 12 18 0 mn L=2 W=8
M21 0 19 21 0 mn L=12 W=80
M25 22 19 0 0 mn L=12 W=80
M27 23 21 0 0 mn L=4 W=75
M28 21 23 19 0 mn L=4 W=75
M24 18 23 22 0 mn L=4 W=75
M32 24 3 18 0 mn L=2 W=8

```

*correspondence between node and phase name

```

* PH2=3
* PH1=6
* PH2D=8
* PH1D=12
* VSS=0
* VDD=11

```

The mn transistor model is defined in the pattern file, and instantiated in the netlist file. Please note that the NQS parameter is zero to prevent problems during transient simulation.

In order to avoid high impedance nodes due to transistor model inaccuracy, every MOS transistor is completed by conductance between its drain and its source, thanks to .GDMSMOS directive.

```

*-----file SIab.nsx-----
*Regulated cascode memory cell
*-----

*clock and biasing V
V11 6 0 PULSE(5 0 0 1.5E-9 1.5E-9 36E-9
75E-9)
V12 12 0 PULSE(5 0 1.5E-9 1.5E-9 1.5E-9
34.5E-9 75E-9)
V14 3 0 PULSE(0 5 1.5E-9 1.5E-9 1.5E-9
33E-9 75E-9)
V31 8 0 PULSE(0 5 1.5E-9 1.5E-9 1.5E-9
34.5E-9 75E-9)
V15 11 0 DC 5
V36 7 0 DC 2
V33 24 0 DC 2.5

*biasing currents
I30 0 19 SIN 0 10E-6 2E6
I37 11 4 DC 100E-6
I18 11 5 DC 15E-6
I20 11 16 DC 15E-6
I22 11 10 DC 100E-6
I29 11 19 DC 100E-6
I26 11 23 DC 15E-6
I23 11 18 DC 100E-6

*Transistor model
.MODEL MN NMOS LEVEL=5 LUNIT=1U NQS=0
+ COX=1.38E-15 GAMMA=0.59 THETA=0.11
+ PHI=0.73 CJ=130E-18 MJ=0.53 PB=0.68
+ CJSW=600E-18 MJSW=0.53 RSH=55
+ CGBO=500E-18 CGDO=250E-18 CGSO=250E-18
+ JS=12E-18 DL=-0.3 DW=-0.2 AF=0.85
+ KF=1.5E-24 LAMBDA=0.5 WETA=0.6
+ LETA=0.2 VTO=0.69 KP=65U LDIF=1.5

* Analysis requests
.TRACE TRAN {IIN = I(I30)}
.TRACE TRAN {IOUT = I(V36)}

.OP EPS_V=1u VMIN=-1 VMAX=6 DELTAV=100m
EPS_I=100p MAXITER=500 MONITOROP=YES
.TRAN 500E-12 1E-6 0
.H 1E-009 1E-017 1E-008 0.25 2
.GDMSMOS 1E-016
.GBDSMOS 1E-015

```

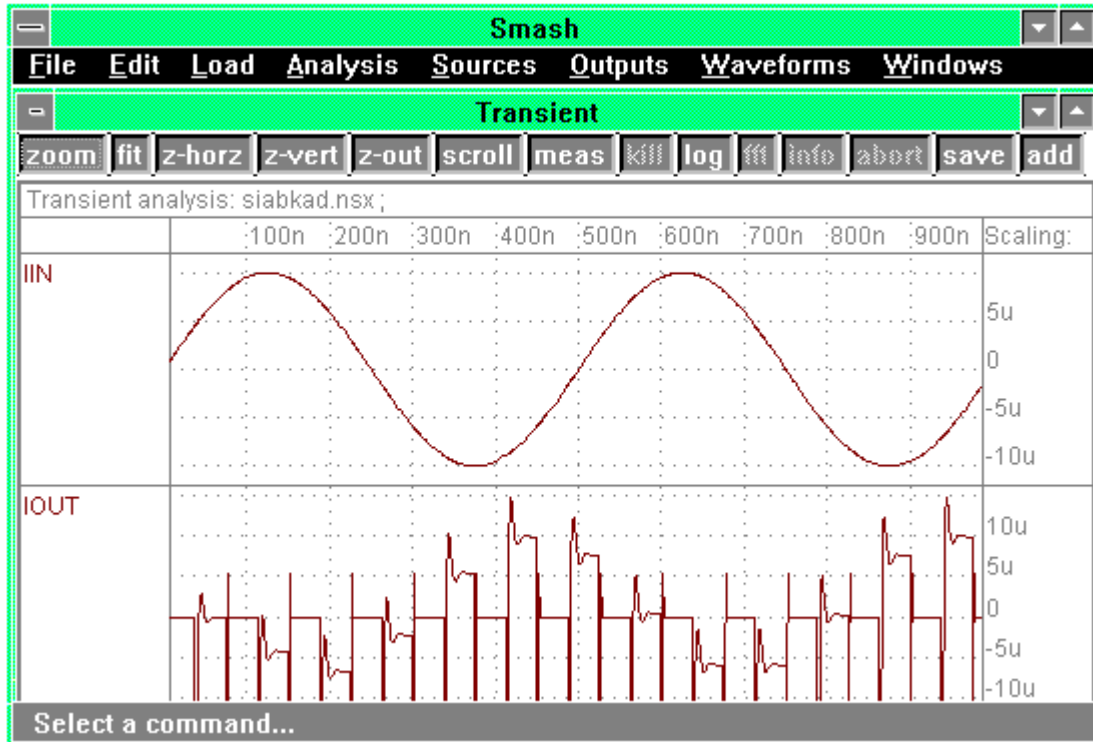


Figure 3 - Input and output current for a regulated-cascode memory cell.

4 - Example 2 - S^2I track-and-hold cell, weak/moderate inversion

Figure 2 presents an S^2I class AB low-power track-and-hold cell. In this example, since the currents involved are relatively low, and because we operate the transistors around the transition from weak to strong inversion [9], the use of standard SPICE models would render convergence impossible with the precision requirements that we have set, making the use of the EKV or other SMASH™ fully continuous model mandatory. It should also be noted that in this example we do not have fully non-overlapping clocks as in the previous case but we make use of the .PARAM feature in SMASH™ to conveniently achieve the best partial overlapping clocks so that charge injection errors are minimized. .PARAM can also be used to optimize device sizes or as an easy way to change many values in a netlist by modifying just a few lines.

The simulation results presented here are for the case of a single-ended class AB S^2I cell ($I_{lim}=1\mu A$, $V_t=0.5V$ [9]), not cascoded, demonstrating the feasibility of the principle and showing how SMASH™ can be effectively used in this problem. Error signals can be attenuated by using a differential structure and even further by using a memory cell based on weakly-inverted differential-pair memory transistors. It should be noted that the circuit has potential to operate at extremely low voltages, the only limitation being the switches. Simulation times are generally high when we ask for such precision levels but once a cell has been optimized its behavior could be represented in SMASH™ at a higher level either as a macro-model or using the C language.

```

*-----file s2iab.nsx-----
* Class AB S2I Cell
*-----

m1 2 2 0 vbn nch l=lmn w=wmn
m2 5 2 6 vbn nch l=lmn w=wmn
m3 3 3 0 vbp pch l=lmp w=wmp
m4 7 3 6 vbp pch l=lmp w=wmp
m5 13 12 4 vbp pch l=lmp w=wmp
m6 9 8 40 vbn nch l=lmn w=wmn
m7 16 15 4 vbp pch l=lmp w=wmp
m8 17 18 40 vbn nch l=lmn w=wmn
msw1 4 p2 5 vswbn nch l=lsn w=wsn
msw2 4 p2r 5 vswbp pch l=lsp w=wsp
msw3 40 p2 7 vswbn nch l=lsn w=wsn
msw4 40 p2r 7 vswbp pch l=lsp w=wsp
msw5 12 pla 5 vswbn nch l=lsnm w=wsnm
msw6 12 plar 5 vswbp pch l=lspm w=wspm
msw7 13 plad 5 vswbn nch l=lsn w=wsn
msw8 13 pladr 5 vswbp pch l=lsp w=wsp
msw11 9 plad 7 vswbn nch l=lsn w=wsn
msw12 9 pladr 7 vswbp pch l=lsp w=wsp
msw13 8 pla 7 vswbn nch l=lsnm w=wsnm
msw14 8 plar 7 vswbp pch l=lspm w=wspm
msw15 13 plb 10 vswbn nch l=lsn w=wsn
msw16 13 plbr 10 vswbp pch l=lsp w=wsp
msw17 10 plb 9 vswbn nch l=lsn w=wsn
msw18 10 plbr 9 vswbp pch l=lsp w=wsp
msw19 13 p2 14 vswbn nch l=lsn w=wsn
msw20 13 p2r 14 vswbp pch l=lsp w=wsp
msw21 14 p2 9 vswbn nch l=lsn w=wsn
msw22 14 p2r 9 vswbp pch l=lsp w=wsp
msw23 15 plb 5 vswbn nch l=lsnm w=wsnm
msw24 15 plbr 5 vswbp pch l=lspm w=wspm
msw25 16 plbd 5 vswbn nch l=lsn w=wsn
msw26 16 plbdr 5 vswbp pch l=lsp w=wsp
msw27 17 plbd 7 vswbn nch l=lsn w=wsn
msw28 17 plbdr 7 vswbp pch l=lsp w=wsp
msw29 18 plb 7 vswbn nch l=lsnm w=wsnm
msw30 18 plbr 7 vswbp pch l=lspm w=wspm
msw31 16 p2 14 vswbn nch l=lsn w=wsn
msw32 16 p2r 14 vswbp pch l=lsp w=wsp
msw33 14 p2 17 vswbn nch l=lsn w=wsn
msw34 14 p2r 17 vswbp pch l=lsp w=wsp
cin 6 40 lp
cout 14 19 lp
rout 19 0 50e4
re 6 10 1e-3
rp 4 rsp 50
cp 4 rsp 15p
rm 40 rsm 50
cm 40 rsm 15p

```

Please note that the convergence analysis (directive .OP) is achieved with basic options, once the voltage range [-1;1] is given.

Transistor models (nmos and pmos) are described in the pattern file and their size are given in the .PARAM directive in order to easily adapt parameters.

```

*-----file s2iab.pat---
* Class AB S2I Cell
*-----

* parameters
.PARAM I=300n VDD=1 IB1=20n IB2=20n
+mu=lu
*switches are biased at (VTO +0.4V)
+ VTOP=-0.53 VTON=0.49
+ VL='VTOP-0.4' VH='VTON+0.4'
+ TR=3n TF=3n T=20E-6
*transistor size
+ LMN='5*mu' LMP='5*mu' WMN='17*mu'
+ WMP='64*mu'
+ LSN='1.6*mu' LSP='1.6*mu'
+ LSNM='1.6*mu' LSPM='1.6*mu'
+ WSN='1.6*mu' WSP='4.4*mu'
+ WSNM='1.6*mu' WSPM='4.4*mu'

* input current
IIN 6 0 SIN 0 I '1/(T*10)'
* input bias
IB1 4 2 IB1
IB2 3 40 IB2
VPLUS rsp 0 'VDD/2'
VMINUS rsm 0 '-VDD/2'
* output bias
VDUM 14 19 DC 0
* bulk connections
VVSWP VSWBP 0 DC 'VDD/2'
VVSBN VSWBN 0 DC '-VDD/2'
VVBV VBP 0 DC 'VDD/2'
VVBV VBN 0 DC '-VDD/2'

*analysis request & options
.OP EPS_V=1u VMIN=-1 VMAX=1 DELTAV=182m
+ EPS_I=100p MAXITER=500 BIASINFO=LONG
+ MODELINFO=YES

.CAPAMIN 10E-015

.EPS 500n 100m 100p
.H 2n 10f 100n 250m 2
*.TRAN 'T*0.01' 'T*12' 0
.TRAN 200n 240u 0

* EKV Model transistor NMOS and PMOS
.MODEL NCH NMOS LEVEL=5
+ COX=2.3e-3 VTO=0.49
+ GAMMA=0.55 PHI=0.5 KP=107u
+ THETA=0.071 UCRIT=1.65e6
+ DL=-0.5e-6 DW=-0.26e-6
+ RS=57.5 RD=57.5
+ JS=0.01e-03
+ CJ=364e-6 CJSW=115e-12
+ CGDO=192e-12 CGSO=192e-12
+ CGBO=144e-12
+ LDIF=1.4u

.MODEL PCH PMOS LEVEL=5
+ COX=2.3e-3 VTO=-0.53
+ GAMMA=0.6 PHI=0.3 KP=38e-6
+ THETA=0.136 UCRIT=3.26e6
+ DL=-0.32e-6 DW=-0.29e-6
+ RS=125 RD=125
+ JS=0.038e-03
+ CJ=670e-6 CJSW=460e-12
+ CGDO=192e-12 CGSO=192e-12
+ CGBO=144e-12
+ LDIF=1.4u

```

With the same idea, the different phases command signals are described thanks to parameters VL VH TF TR and T.

The simulation displays signals IOUT and IIN in one graph and the different phases command on the second graph. Note that the signal displayed can be a combination of different signals. See the add formula function in the SMASH™ documentation.

```
* clock generation
VPHI1A P1A 0 PULSE VL VH TF TR TF '(T-
10*TF-4*TR)/4' T AC 0
VPHI1AR P1AR 0 PULSE VH VL TF TR TF '(T-
10*TF-4*TR)/4' T AC 0
VPHI1AD P1AD 0 PULSE VL VH TF TR TF '(T-
6*TF-TR)/4' T AC 0
VPHI1ADR P1ADR 0 PULSE VH VL TF TR TF
'(T-6*TF-TR)/4' T AC 0
VPHI1B P1B 0 PULSE VL VH
'(T+3*TR+2*TF)/4' TR TF '(T-10*TF-
4*TR)/4' T AC 0
VPHI1BR P1BR 0 PULSE VH VL
'(T+3*TR+2*TF)/4' TR TF '(T-10*TF-
4*TR)/4' T AC 0
VPHI1BD P1BD 0 PULSE VL VH
'(T+2*TF+3*TR)/4' TR TF '(T-6*TF-
7*TR)/4' T AC 0
VPHI1BDR P1BDR 0 PULSE VH VL
'(T+2*TF+3*TR)/4' TR TF '(T-6*TF-
7*TR)/4' T AC 0
VPHI2 P2 0 PULSE VH VL 0 TR TF '(T-
2*TF)/2' T AC 0
VPHI2R P2R 0 PULSE VL VH 0 TR TF '(T-
2*TF)/2' T AC 0

* screen
.TRACE TRAN {IOUT = I(VDUM)} {IIN =
I(IIN)}
.TRACE TRAN {PHI2 = V(P2)}
```

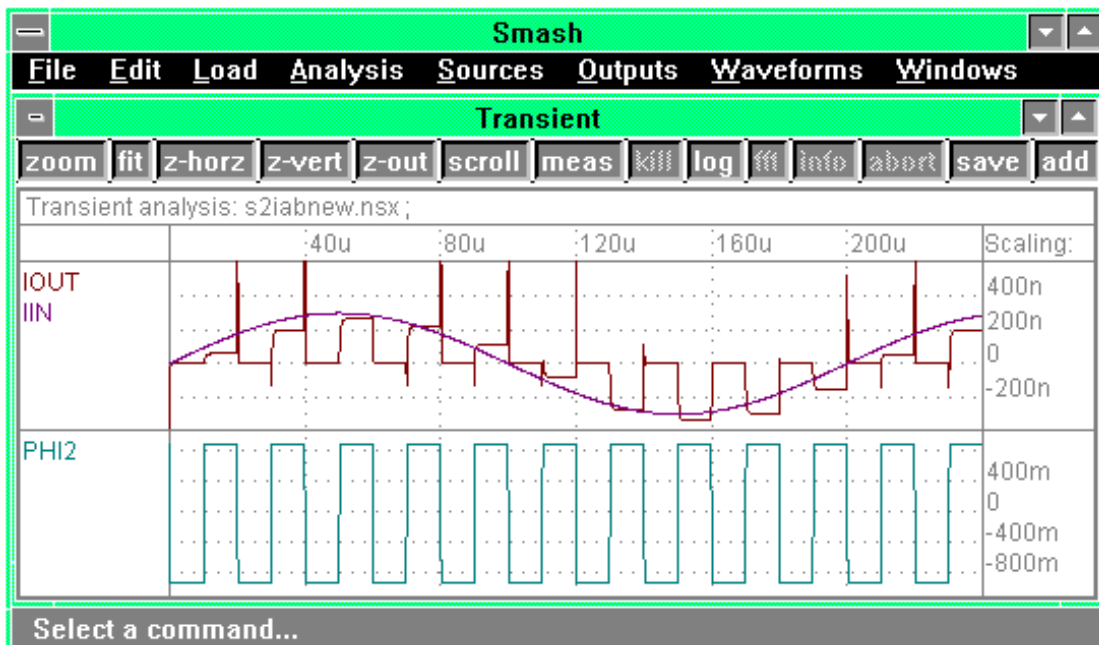


Figure 4 - Input, output, and clocking scheme in a low-power class AB track-and-hold S^2I cell [9].

5 - Issues on higher-level modeling

The optimization of an SI building block should be made at the transistor level but at the system level simulating large systems can become very time-consuming. In this case two approaches can be adopted for higher level simulation. In a first step, the behavior of a circuit can be estimated by building macro-models of its cells as illustrated in figure 5.

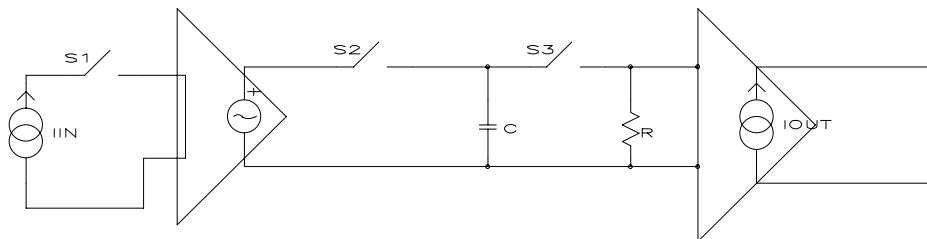


Figure 5 - Macromodel of an SI cell

The model operates as follows. On the sampling phase ϕ_1 the switches S1 and S2 are closed and S3 is opened. The capacitor C is charged by the current-controlled voltage source to a voltage V which corresponds to the current I_{in} . During the retrieval phase ϕ_2 , S3 is closed and S1 and S2 are opened. This makes the capacitor C hold the voltage V. R represents the finite output conductance of the cell and other effects such as leakage. By the action of the voltage-controlled current source the output current I_{out} becomes the half-delayed version of the input current I_{in} .

6 - Conclusion

We have illustrated with examples how SMASHTM can be used in a very flexible and straightforward way to simulate SI-based systems. The EKV MOS model and its usage have been summarized and the basic concepts of modern SI cells have been presented together with options needed for their simulation. Tips for good SI simulation practice have been introduced.

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