AMPLIFIERS MACRO-MODELING

Version 1 - May 1995

TABLE

Introduction

The purpose of this application note is to present different modeling approaches with the SMASH^{TM} simulator, illustrated with the choice of amplifier model within a simple application, namely the amplifier gain control. The application context is briefly reviewed and we then focus our attention on the modeling.

In order to decode DTMF signals of small amplitude, the gain of the amplifier has to be controlled. The input signals (IN) of the circuit have to be decoded according to their frequency. The trouble is that their amplitudes (from -45dBm to -4dBm) are too small to be detected by the decoder. Indeed the chosen decoder can only detect signals of at least -32dBm, up to -4dBm.

A logic command (CMD), resulting of the input signal treatment, is therefore necessary to have a gain of approximately 15dB (with a 2dB margin) for the small amplitude signals (from -45dBm to at least -32dBm), and a unity gain in other cases.

The gain control is achieved by altering the feedback resistor of the operational amplifier as detailed in the circuit principle.

Circuit principle

As previously described, the amplifier gain must depend on the CMD command signal. The aim is to produce a gain of 15dB when the command is high (CMD=1) and a unity gain otherwise (CMD=0).

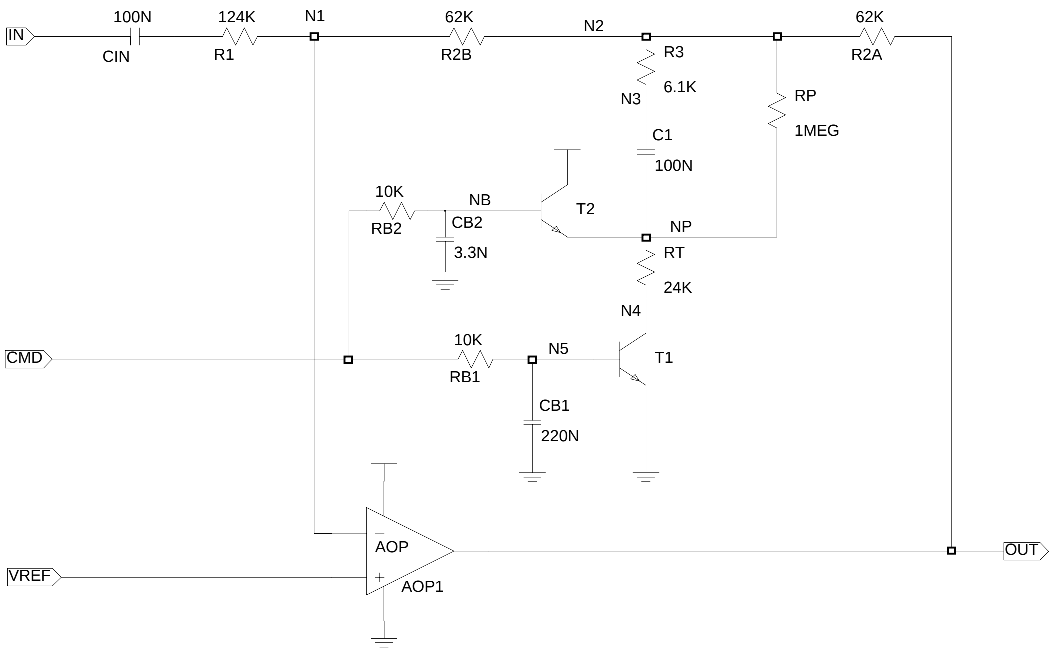


Figure 1 : Amplifier gain control

This function is achieved thanks to two npn bipolar transistors. The former is connected in emitter common mode and acts as a switch (transistor T1), when the latter, connected in collector common mode behaves like a follower (transistor T2).

Unity gain

When the command is zero, the base currents of the transistors are zero and transistors are « off ». The bias of T1 transistor is set by the resistor RP. This transistor behaves like an open switch, isolating the R3 resistor (figure 1).

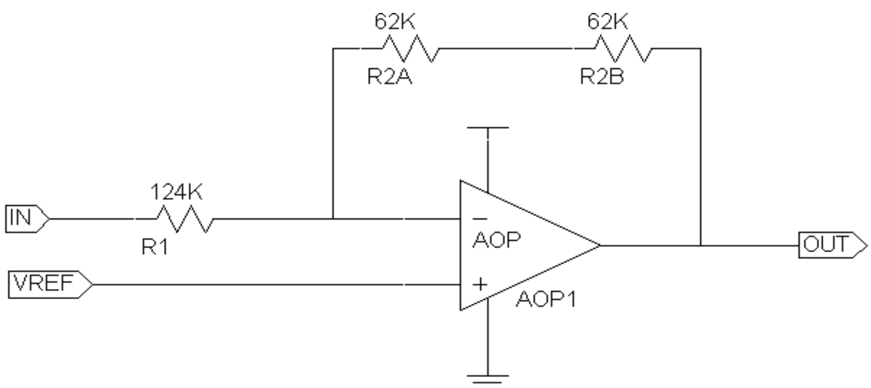


Figure 2 : Small signal schematic for unity gain

The gain expression is $\frac{Vout}{Vin} = -\frac{R2A + R2B}{R1}$, which is 1 if R2A=R2B=R1/2.

Gain for small amplitude signals

When the input signal amplitude is too small to be detected by the decoder, the CMD command is high and brings the transistors in saturation mode. The transistor T1 now behaves like a closed switch and connects the R3 resistor (R3<<RP).

The capacitor C1 cuts down DC disturbances of the control circuit. The purpose of the transistor T2, as a follower, is to bring the voltage on the NP node up to VCC (the base-emitter junction have merely no consequence).

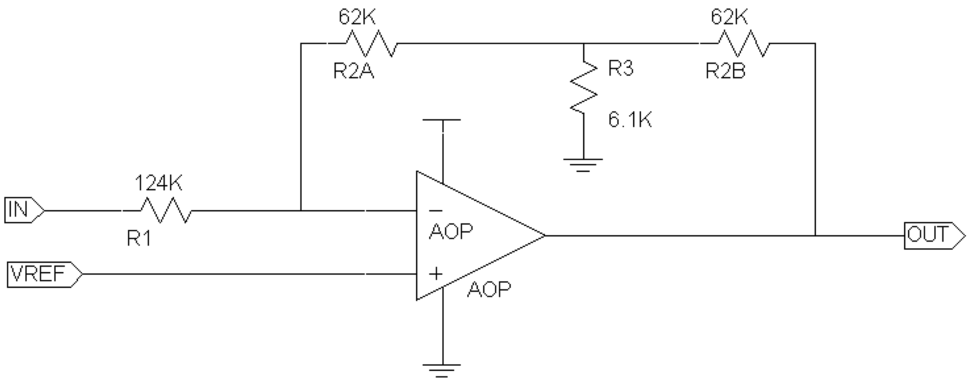


Figure 3 : Small signal schematic

The gain expression is now $\frac{Vout}{Vin} = -\frac{R2A*R2B}{R3*R1} - \frac{R2A+R2B}{R1}$

and with the chosen values, the gain $G = 1 + \frac{R1}{4*R3} \approx 6.08$ (≈15dB).

We have seen the gain control principle with a logical command, assuming that the amplifier is ideal. We now will study different models and analyze the associated simulations.

Models and simulations

First, we will examine the input files for SMASH™. The cga.nsx and cga.pat files contain (resp.) the description of the circuit (the netlist) and the simulation directives, including stimuli.

```
*-----------------------------------
* NETLIST FILE CGA.NSX.
*-----------------------------------

** Global (used) nets:
**  VSS
**  VCC

  CIN       N0 IN 100N
  R1        N1 N0 124K TC=0

*feedback resistor
  R2B       N2 N1 62K TC=0
  R2A       OUT N2 62K TC=0
*added resistor when T1 is on.
  R3        N2 N3 6.1K
  RP        N2 NP 1MEG
  C1        N3 NP 100N

* transistor T2, follower.
  RB2       NB CMD 10K TC=0
  CB2       NB VSS 3.3N
  QT2       VCC NB NP NPNMOD

* transistor T1, switch.
  RT        NP N4 24K
  RB1       N5 CMD 10K TC=0
  CB1       N5 VSS 220N
  QT1       N4 N5 VSS NPNMOD

* amplifier.
*1/Ideal model with voltage source
*Eop1 OUT 0 VREF N1 1000
*2/Model with transfer function:
*Xop1 VREF N1 VCC VSS OUT \ 1000 AMPLI
*3/National Semiconductor model:
*Xop1 VREF N1 VCC VSS OUT TLC27L4

RIN IN VSS 1K
RCMD CMD VSS 1K
ROUT OUT VSS 1K
```

```
*-----------------------------------------
* PATTERN FILE CGA.PAT
*-----------------------------------------

* SOURCES
V_VCC VCC 0 3.6
V_VREF VREF 0 1.7
VIN IN 0 SIN( 0 100M 700 0 0 0 ) AC 1 0
VSS VSS 0 0
* Command at high level
*V_CMD CMD 0 PWL 0 3.6 4M 3.6 4.1M 0
* Square command (0-1-0)
V_CMD CMD 0 PWL 0 0 4M 0 4.1M 3.6 14M 3.6
14.1M 0

*Simple transistor model
.MODEL NPNMOD NPN

*LIBRARY
.LIB .\AMPLI\AMPLI.CKT
.LIB .\ELECT\TLC27L4.CKT


*SCREEN
.TRACE  AC     VDB(OUT) VDB(IN)
.TRACE  TRAN   V(CMD) V(IN) V(OUT)

.OP EPS_V=1U VMIN=-200 VMAX=200
DELTAV=100M EPS_I=100P MAXITER=500

.AC DEC      10 10 10MEG
.EPS         10U 100M 1N
.H           5U 1F 10U 250M 2
.TRAN        60U 20M 0
```

Three types of amplifier model will be considered, as described in the netlist file:
- an ideal model using a controlled voltage source,
- a subcircuit describing an ideal amplifier transfer function,
- a subcircuit describing an electrical model of an amplifier.

Input signals are imposed by our application as follows:
- VCC, the supply voltage equals to 3.6V,
- VREF, the input reference signal of the amplifier is of 1.7V,
- VIN, the input signal is a sinusoidal source with frequency of 700Hz, and could be a telephone signal.

Ideal model with a voltage source

We now consider the ideal case, where the amplifier is modeled with a simple gain of 1000. The corresponding description line in the netlist file for this very simple model is:

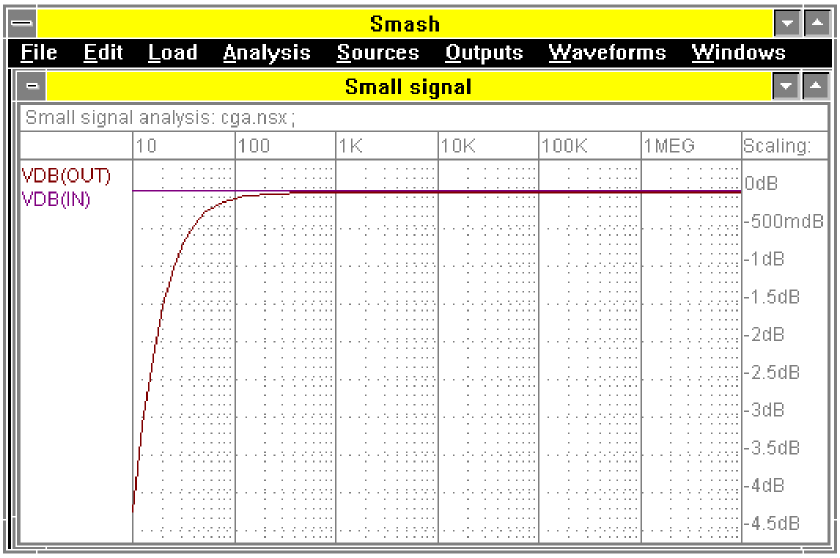
`Eop1 OUT 0 VREF N1 1000.`

We will successively run three analysis to study each amplifier model. First, two 'small signal' analysis on the IN signal (`VIN IN 0 SIN( 0 100M 700 0 0 0 ) AC 1 0`), with different CMD signal and we then display the transient analysis.

- Small signal analysis with CMD command signal at zero (V_CMD CMD 0 PWL 0 0 4M 0 4.1M 3.6 14M 3.6 14.1M 0). The gain of the OUT signal must be 0dB, as explain in the principle part.
- Small signal analysis with CMD command signal at high logical level (V_CMD CMD 0 PWL 0 3.6 4M 3.6 4.1M 0). The OUT signal gain is theoretically at 15dB.
- Transient analysis with a square command signal CMD in order to clearly show the transitions of the OUT signal when CMD changes.

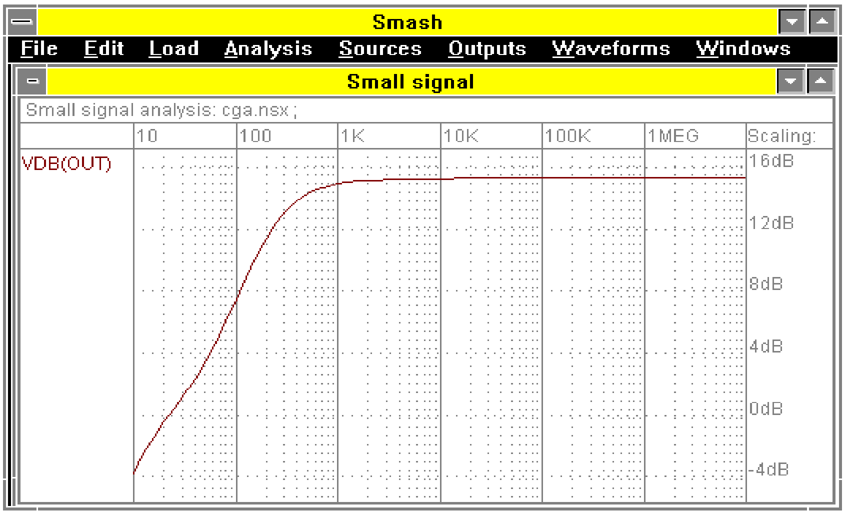
Here are the results of these simulations for our ideal model.

AC analysis with CMD at zero :



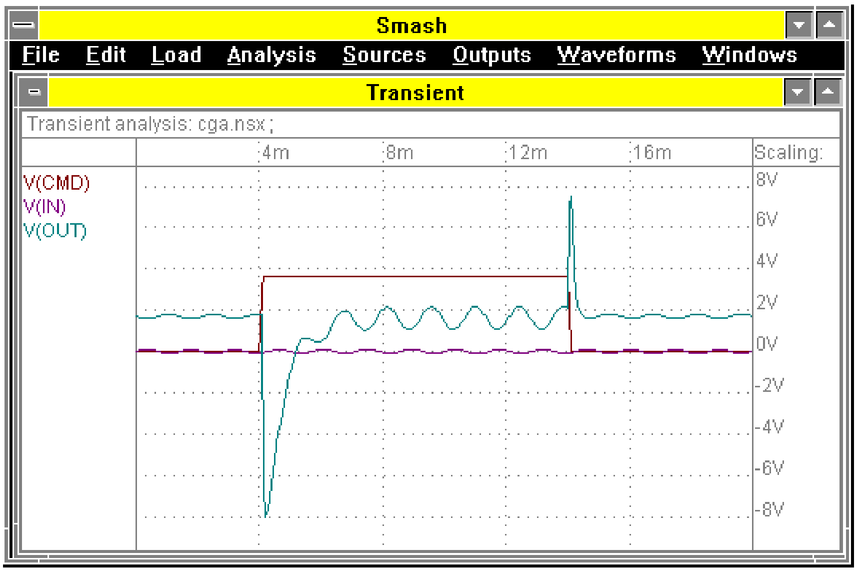
Circuit exhibits unity gain for frequency larger than 100Hz.

AC analysis with CMD high :



Circuit exhibits 15dB gain for frequency larger than 1KHz.

Transient analysis :



The input signal (sinusoidal signal centered on 0V) is amplified when the square command signal is at high logical level (3.6V). The command signal triggers the transitions on the OUT signal. As the ideal model amplifier does not take saturation into account, the OUT signal amplitude reaches high values (-8V to 8V), which are not realistic.

Amplifier model with transfer function

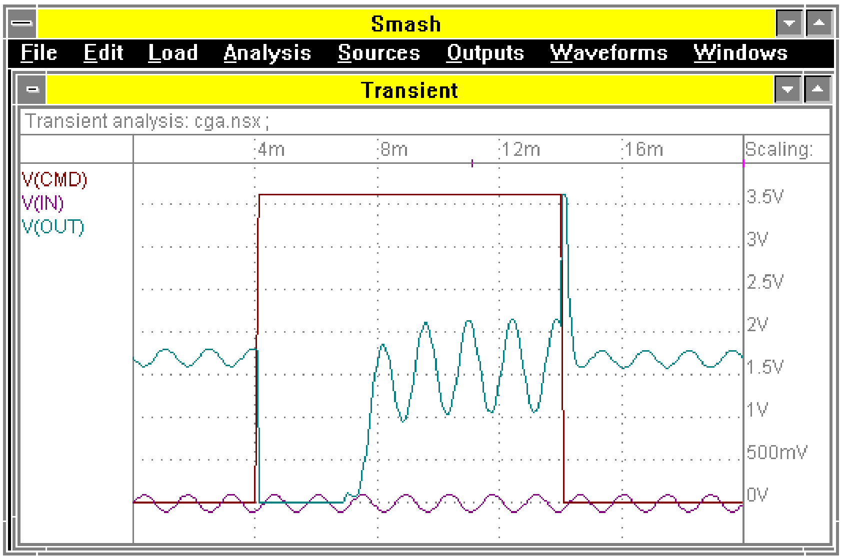
We now consider the following model, called in the netlist file with the expression
`Xop1 VREF N1 VCC VSS OUT \ 1000 AMPLI`

```
*------------------------------- AMPLI.CKT------------
.SUBCKT AMPLI EP EM VDD VSS S \ GAIN

G1 VSS 1 EP EM GAIN
R1 1 VSS 1

G2 vss 2
+ IF { V(1) >= V(VDD) }
+ THEN { V(VDD) }
+ ELSE { 0 }
R2 2 VSS 1

G3 VSS 3
+ IF { V(1) <= V(VSS) }
+ THEN { V(VSS) }
+ ELSE { 0 }
R3 3 VSS 1

G4 VSS 4
+ IF { ABS(V(1)-(V(VDD)+V(VSS))/2 ) < ((V(VDD)-V(VSS))/2) }
+ THEN { V(1) }
+ ELSE { 0 }
R4 4 VSS 1
ES S VSS VALUE { V(2)+V(3)+V(4) }
.ENDS
*----------------------------------------------------------
```

This model, a more realistic one, makes use of non-linear controlled sources (G2, G3 and G4) to implement the output saturation. Notice the usage of a conditional form (IF, THEN, ELSE).

Its small signal behavior is the same as in the previous case. Consequently, we will only display the transient analysis for this model.

Transient analysis :



The OUT signal now stays in the [VSS, VCC] range.

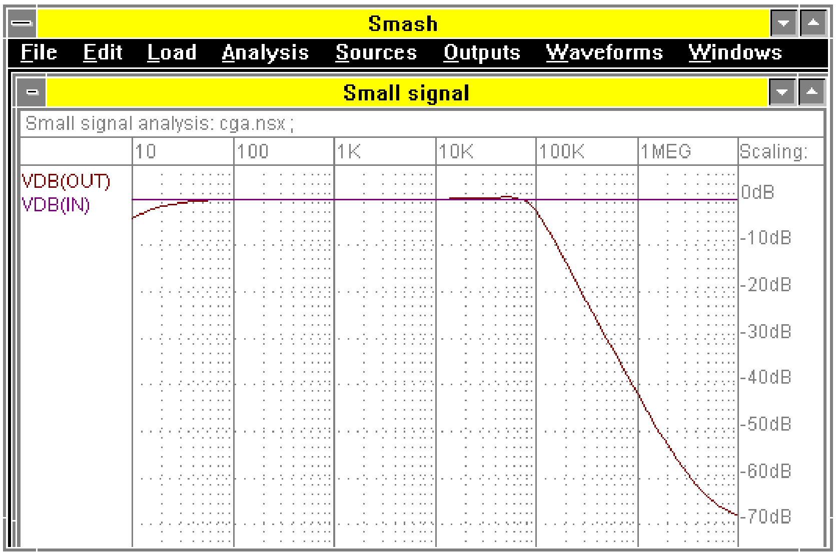
Electrical model of the amplifier

The model described below is supplied by National Semiconductor. It is called in the netlist file with the expression :

```
Xop1 VREF N1 VCC VSS OUT TLC27L4
```

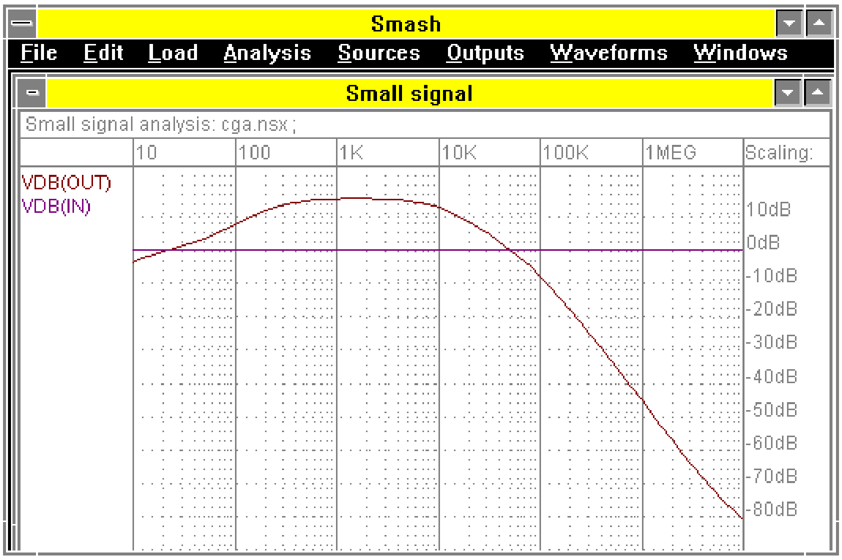
```
* TLC27L4 operational amplifier "macromodel" subcircuit
*
* connections:   non-inverting input
*                | inverting input
*                | | positive power supply
*                | | | negative power supply
*                | | | | output
*                | | | | |
.subckt TLC27L4  1 2 3 4 5
*
  c1   11 12 8.002E-12
  c2    6  7 15.00E-12
  dc    5 53 dx
  de   54  5 dx
  dlp  90 91 dx
  dln  92 90 dx
  dp    4  3 dx
  egnd 99  0 poly(2) (3,0) (4,0) 0 .5 .5
  fb    7 99 poly(5) vb vc ve vlp vln 0 975.8E6 -1E9 1E9 1E9 -1E9
  ga    6  0 11 12 10.37E-6
  gcm   0  6 10 99 146.5E-12
  iss   3 10 dc 600.0E-9
  hlim 90  0 vlim 1K
  j1   11  2 10 jx
  j2   12  1 10 jx
  r2    6  9 100.0E3
  rd1   4 11 96.45E3
  rd2   4 12 96.45E3
  ro1   8  5 85
  ro2   7 99 85
  rp    3  4 689.7E3
  rss  10 99 333.3E6
  vb    9  0 dc 0
  vc    3 53 dc 1.650
  ve   54  4 dc .7
  vlim  7  8 dc 0
  vlp  91  0 dc 20
  vln   0 92 dc 20
.model dx D(Is=800.0E-18)
.model jx PJF(Is=350.0E-15 Beta=200E-6 Vto=0)
.ends
```

AC analysis with CMD=0 :



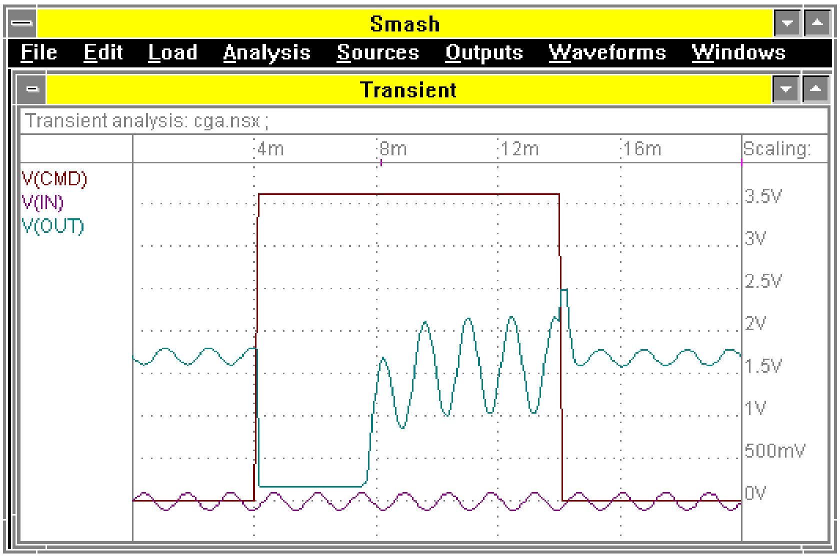
The model is no longer ideal and a gain fall is observed at a certain frequency (≈100KHz). In fact this model is far much realistic than the previous ones, and takes into account not only the saturation problem but also the limitations due to the slew-rate, and the transition frequency in open loop.

AC analysis with CMD=1 :



The gain fall appears for a smaller frequency than with the ideal model.

Transient analysis :



This model exhibits an output saturation of 2.5V.

Simulations comparisons

The table below briefly compares the simulation durations, depending on the chosen model for transient analysis.

	Duration	Transient duration when CMD : 0-->1	Transient duration when CMD : 1-->0
Model eaop (controlled voltage source)	25s	2.85ms	0.67ms
Model ampli (transfer function)	33.5s	4.90ms	0.7ms
Electrical model	46s	4.5ms	1.39ms

One should note that simple model like eaop offers quick simulation, when more complex model such as the electrical one (using diodes and jfet junctions) is slower. Thus a compromise has to be found, between speed and accuracy. When only the qualitative behavior of a circuit is needed, one should always choose simple models first, and then use more accurate models for final simulations.