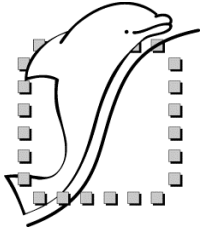


Mixed Signal Virtual Components COLINE, a case study

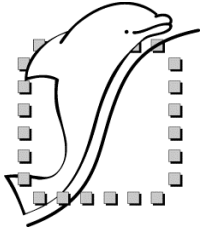
J.F. POLLET - DOLPHIN INTEGRATION
Meylan - FRANCE

<http://www.dolphin.fr>



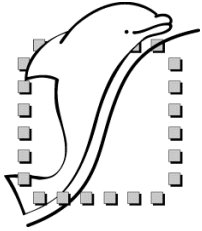
Overview of the presentation

- Introduction
- COLINE, an example of Mixed Signal V.C.
- Dolphin standard deliverables for Mixed Signal V.C.
- Comparison Dolphin deliverables / Mixed Signal VSI specifications
- Customer case study
- IP provider and Customer suggestions for VSI extension
- Conclusion and trends



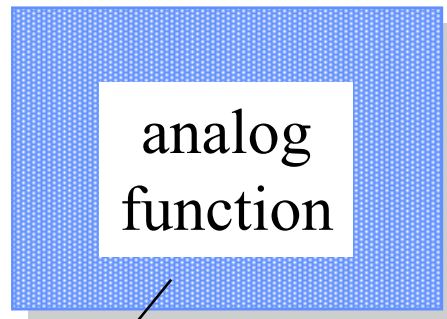
Dolphin Integration as a Mixed Signal V.C. Provider

- Created in 1985 as an independant Design Center
- 13 years of experience in logical and mixed signal designs
- Moved to VC Provider in 1995
- VSIA member since July 1997
- Customer references: NEC, SGS-Thomson, μ EM, TI, Motorola, AMS, ALCATEL, AEROSPATIALE...
- Focus on high perforlances ADC, DAC, codecs, PLLs in 0.5 μ m, 0.35 μ m, 0.25 μ m CMOS processes



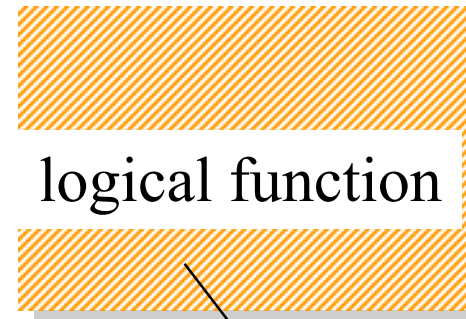
What is a Mixed Signal VC?

Hard VC

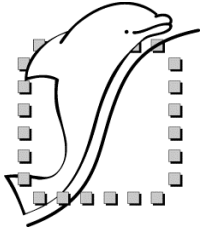


transistors, resistors
capacitors

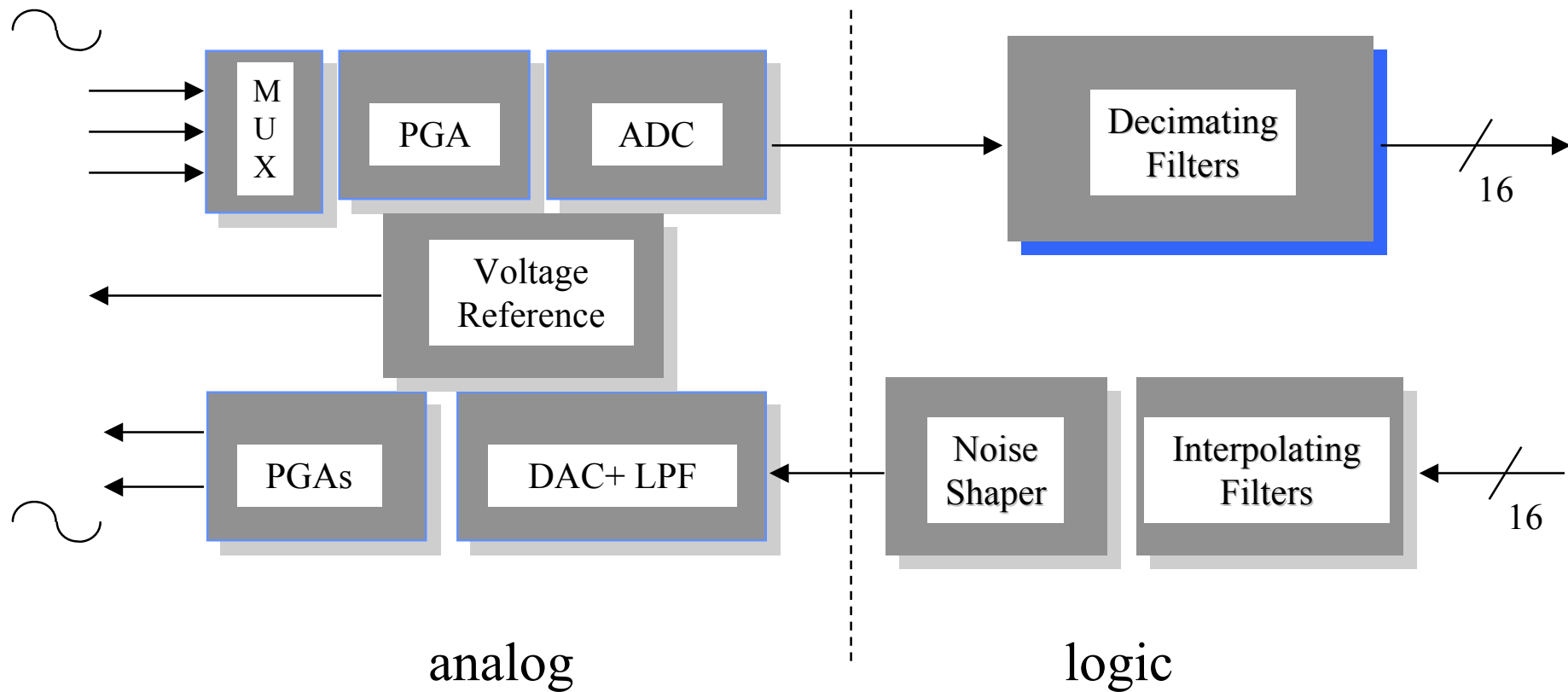
Soft VC

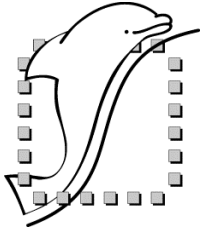


with complexity
from some hundred
to several 10k gates



COLINE, Analog Front End for modems, fax, audio





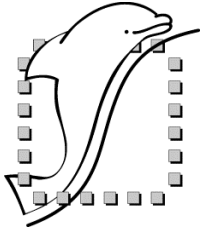
COLINE Characteristics

■ Main features

- Single power supply $3.3\text{ V} \pm 10\%$
- Sampling frequency bandwidth from 4 kHz up to 48 kHz
- Filters compatible with G714 UIT recommendation
- Power down mode, test modes offering different loops
- Calibration mode in ADC for offset cancellation

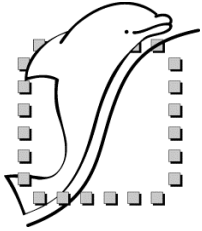
■ Performances

- SNR and THD $> 80\text{ dB}$
- Low power consumption: typically 10 mW @ 8 kHz sampling frequency
- Two existing versions optimized for 8 kHz and 9.6 kHz sampling frequency



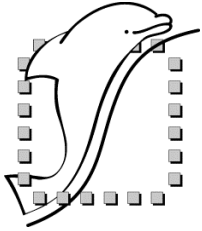
COLINE Characteristics

- 16 bit delta-sigma ADC and DAC
- Additional analog functions
 - Internal Voltage Reference
 - Analog input multiplexing
 - Analog programmable gain amplifiers on inputs: -6 dB up to 24 dB
 - Programmable gain attenuators on outputs: -30 dB up to 0 dB
- Retargetable toward any 3.3 V submicron CMOS process
 - Pure digital process for the ADC + DAC
 - With resistor and capacitor mask layers for the additional analog functions



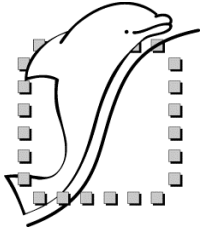
COLINE Characteristics

- Patented and silicon proven Operational Amplifier for switched capacitors filters: low noise, low power, low silicon area
- Silicon complexity
 - With a 0.35 μm CMOS process, three metal mask layers, one resistor and one capacitor mask layer
 - 0.25 mm^2 for the ADC + DAC
 - 2.4 mm^2 for the complete analog part
 - 14 000 gates for the digital part



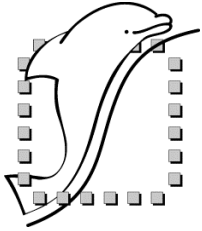
Dolphin standard deliverables for Mixed Signal V.C.

- Logical part (soft VC)
 - VERILOG RTL synthesizable model
 - VERILOG testbench
 - synthesys and simulation scripts
 - Functionnal and industrial test patterns
- Analog part (hard VC)
 - SPICE netlist
 - GDSII data base
 - Industrial test specification
 - Schematics (optional)
 - Behavioral models and REPACK (on request)



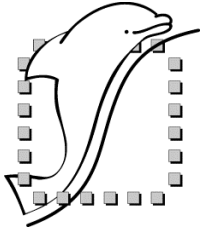
Dolphin standard deliverables for Mixed Signal V.C.

- Common deliverables for logical and analog parts
 - Specifications: description of the pins, the working modes, the electrical characteristics (29 pages for COLINE)
 - User's guide (22 pages for COLINE + appendixes)
 - Validation plan for the prototypes of a test circuit (on request) (38 pages for COLINE)
 - Evaluation board specification and user's guide (on request) (40 pages for COLINE)
 - Mixed signal behavioral model (on request)
 - Training / support / hot fax hot email/ yield support (on request)



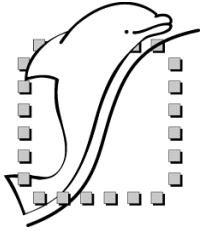
Comparison Dolphin deliverables versus VSI specifications

- Comparison has been done afterwards
- Difference in the document structure
- “M” items have been delivered except for
 - 2.1.3 Verification of Claims (digital only have been provided)
 - 2.5 Test requirements: document, not files
- Improvement of our user guide after VSI specification analyse
 - 2.1.6 Application notes (R)
 - 2.A1 Process definition



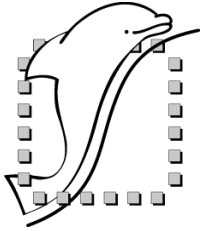
Customer case study

- Customer = NEC Electronics, Europe ASIC Division
- Process: 0.35 μm CMOS, with a special capacitor and a special resistor mask layers
- Design work made by Customer :
 - DRC verification of the analog layout data base
 - logical synthesys and place and route of the logical data base
 - assembly analog/logical
 - test circuit generation and fabrication
 - insertion in ASIC block library



Customer case study

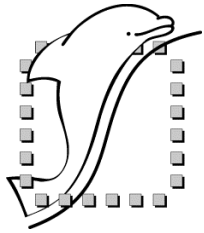
- Two major constraints for IP provider:
 - respect some features of the Customer internal ASIC design flow
 - I/O pitch
 - special design rules for analog input/output protections
 - internal specific test-bus for logical functions
 - specific functions and constraints required by the first application ASIC
 - predefined pinout
 - additionnal functions (mainly logical)



Customer case study

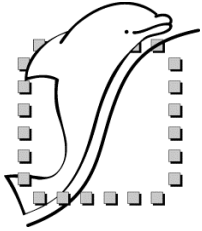
■ Consequences

- For the analog part
 - New floorplan and layout of the analog part
 - Specific redesign of output stages buffers
- For the logical part
 - addition of a logical interface between specific test bus and the COLINE VC input/output logical I/Os
 - edition of a specific “test-bench”
- For both analog and logical parts
 - edition of a specific “user guide”
 - specific Mixed signal simulations



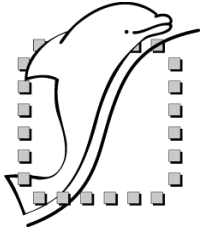
Customer and Provider suggestions for improving VSI specifications - 1

- Strong request for 2.3.A7- Prototype evaluation method
 - Are highly recommended, especially for a complex VC like COLINE
 - insertion of the VC in a test circuit for evaluations
 - delivery of an evaluation board
 - specification and user's guide of such an evaluation board
 - Characterization plan of test circuit prototypes
 - requested and delivered for COLINE



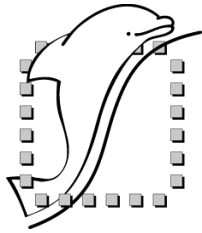
Customer and Provider suggestions for improving VSI specifications - 2

- Documentation and file at the highest level of the VC with a detailed description of the different blocks and their interconnections
- Example of integration of the VC with external function:
 - document describing the rules to follow and the design methodology
 - corresponding files if necessary
- Reference voltage
 - CMOS reference voltage use parasitic bipolar transistor, not characterized
 - the way of tuning this reference has to be specified in the user guide



Differences with the development of an application specific macrocell

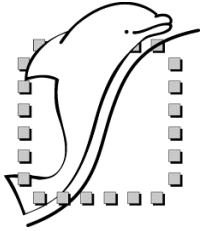
- VC provider point of view
 - VC specifications cover items not always required by the customer
 - application notes: Customer intends to use the VC in configurations for which it had not been specified e.g.
 - special usage of stand-by modes
 - changing the sampling frequencies ”on the fly”
 - more documentation required
 - difficult to imagine if and where the integrator will have or not some difficulties
 - e.g. assembling the analog and logical parts
 - specific developments for insertion in a particular design flow
 - additional requirements for an ASIC library (compared to an ASSP)



Differences with the development of an application specific macrocell

■ Customer point of view

- specific requirements not covered by the original VC specifications, e.g.
 - lower power supply voltage than specified
 - special clock signal characteristics: must adapt the ASIC to the characteristics of the VC
- ask for additional functions or VC design modifications (case of digital filters and PLL for COLINE)
- better time-to-market



Conclusion and Trends

- Interests in VSI Specifications
 - Guide and reference
 - Standardisation will increase the business
- Most important requirements for extensions of mixed signal VC specification
 - models of analog and mixed-signal VC:
 - Necessity of specification of the level of refinements
 - what kind of models want the users? at which step of the design?
 - Intensive work and suggestions for mixed-signal industrial test, a bottleneck for the time to market