COMON - The European Compact Modeling Network

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Abstract — **COMON is the European FP7 Marie-Curie project "Compact Modeling Network" which brings together 15 European universities and companies in an attempt to transfer the scientific and technological knowledge from academia to industry, to strengthen local, European integrated circuit (IC) design capabilities with powerful modeling and CAD methodologies and to achieve integration of European research in fragmented R&D areas for the benefit of both young and experienced researchers. The MOS-AK/GSA Group provides compact modeling Verilog-A standardization platform as well as the international dissemination support.**

Index Terms — **Compact modeling, SPICE, Verilog-A, analog/RF IC CMOS, multiple-gate MOSFET, IIIV HEMT, HV MOSFET, Monte-Carlo analysis, statistical modeling**

I. Introduction

THE Compact Modeling Network (COMON) [1] is a consortium of 15 European universities and companies, which came together in an attempt to transfer the scientific and technological knowledge from academia to industry, to strengthen local, European integrated circuit (IC) design capabilities with powerful modeling and CAD methodologies and to achieve integration of European research in fragmented R&D areas for the benefit of both young and experienced researchers. The global structure of the project, presented in this paper, is divided into Working Groups (WGs), each one addressing one specific type of devices: Multiple-gate MOSFETs (WG1), High Voltage MOSFETs (WG2) and advanced III-V HEMTs (WG3). In parallel COMON Work Packages (WPs) focused on related SPICE level modeling and standardization tasks are established. A compact modeling development and parameter extraction workpackage (WP1) addresses the modeling and characterization techniques developed by COMON partners for modeling of the target semiconductor devices including such effects as the thermal effects, RF, noise and microwave behavior as well as the process fluctuations. A compact modeling, implementation and benchmarking workpackage (WP2) is related to the advanced compact models for implementation in open source/GNU and commercial circuit simulators. The model implementation is carried out at higher levels of abstraction using standard VHDL-AMS and Verilog-A description. In the workpackage WP3, entitled "Evaluation and demonstration of the models and design tools on dedicated test chips", a comprehensive evaluation of the compact models by simulating a number of analog, digital, RF circuits for the different available semiconductor technologies are considered. The test chips will be fabricated by the industrial COMON partners. A dissemination, training, exploitation and IPR management workpackage (WP4) addresses the dissemination of COMON modeling results which is to be performed through scientific publications in international journals, presentations at conferences, and maintenance of COMON web site. A series of the workshops on compact modeling (MOS-AK/GSA) are also organized twice a year. Training courses and summer schools are planned as well. Finally, within the project management workpackage (WP5) the network coordination and administration tasks are done.

II. Multiple-gate MOSFETs

Today, the DG MOSFET is probably the CMOS based 'nano-electron' device that has been modeled the most since the first work published by Taur [2], more than 10 years ago. In particular, analytical modeling (compact modeling) of the undoped symmetrical DG MOSFET has been investigated in many details [3]-[6], including advanced features such as short channel effects and quantum mechanical corrections [7]-[10]. On the other hand, less work has been done on double gate devices with doped channels. The models in [5],[11] assume a highly doped DG MOSFET. The model presented in [12]-[15] is valid for a broad range of doping, and as a limit case also for undoped devices, but needs interpolation functions together with an empirical expression for difference of potentials between the surface and the centre of the silicon layer. In [16], the authors propose a model based on the model developed in [4] but introduce some arbitrary approximations to ensure 'continuity' between doped and undoped devices. Even though for matching and mobility considerations the silicon layer should ideally be undoped, many working devices have their channel doped in order to fine tune the threshold voltage. Therefore, a compact model for DG MOSFETs, valid in the practical range of doping concentrations, including undoped devices, is definitely needed. We propose to demonstrate how doping the silicon reverts to define an equivalent silicon film thickness from the point of view of the integrated charge density within the channel, and thus also for the current.

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Validations with TCAD simulations confirm that the 'equivalent thickness' concept is valid until the semiconductor becomes almost undepleted, i.e. when coupling between the gates vanishes, meaning that the DG concept also breaks off. For the same reason, the model may not be valid when the device operates near flat-band conditions since impurities are no longer fully ionized then. Yet, the transition between total and partial depletion in doped DG MOSFETs was addressed by Liu et. al. [17]. In their paper, the authors proposed to combine an iterative approximation method with Pao-Sah's dual integral to calculate the potentials, charges and current with good accuracy, but also requiring some numerical iteration.

The simple and single formalism presented in this paper for doped (fully depleted) and undoped symmetric DG MOSFETs is found to be very accurate, even when doping is beyond the partial depletion criteria reported in [17]. Moreover, this model is particularly suited for multigate MOSFETs analog design issues and it can also be efficiently implemented in electrical simulators.

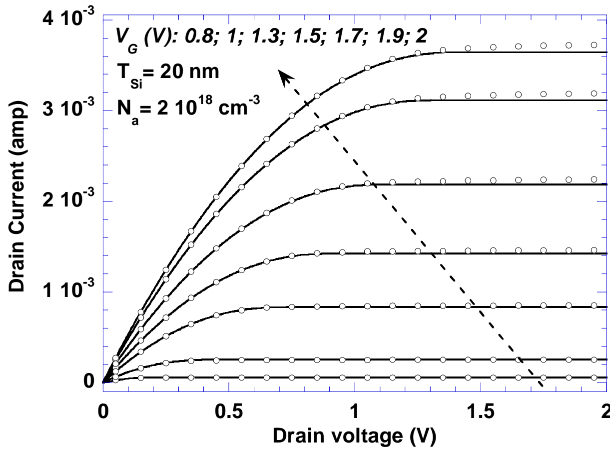

Figure 1. Drain current versus drain voltage for different gate potentials in a 20 nm silicon layer doped at $2\cdot10^{18}$ cm^{-3}; lines: model; dots: TCAD simulations

We propose to evaluate the accuracy of the model with respect to TCAD simulations. In order to get rid of short-channel effects and clearly identify the effects related to the doping, we consider a long channel (1um) double gate MOSFET with a silicon oxide thickness of 1.5 nm, and a constant mobility of 0.1 m^2/Vs. The width was also set to 1um. Doping concentrations and silicon thicknesses are the parameters that will vary along the simulations. A model for the doped DG MOSFET could revert to the undoped one through the definition of an equivalent silicon thickness which depends on the doping concentration. Extensive comparisons with numerical simulations confirm that this approach is valid up to relatively high doping levels, i.e. until the silicon becomes partially depleted, thus setting the basis for a coherent formalism for doped and undoped symmetric DG MOSFETs. Additional work is still required to address quantum mechanical corrections and short channel effects. Furthermore, we expect that this approach may be an interesting basis for compact modeling of doped multigate devices such as GAA and FinFETs.

III. HIGH VOLTAGE MOSFETS

Starting from basic electrostatic equations, we developed an analytical expression for the current that is accurate in all the regions of operation, namely from the weak up to the strong inversion, and from the linear up to the semi-saturated mode. In a first step, the model has been carefully validated with respect to numerical CAD simulations on an idealized structure where all doping profiles and device dimensions where set to typical values. In a second step, the model has also been validated with extensive AMS data provided for commercial HV MOSFET devices. In order to carry out analytical solutions, the problem was thought as 2x1D system instead of a 2 dimensional device. Therefore, we assumed that the HV MOSFET could be simplified into the following topology (Fig.2)

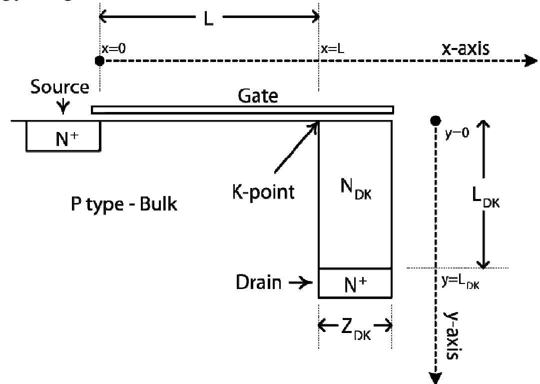

Figure 2. The simplified HV MOSFET topology:

After extensive numerical analysis, an explicit formulation of the current versus applied potential has been obtained. As can be seen on the figures 3 and 4 below, the overall agreement is indeed very satisfactory. The model is able to simulate long and short channel HV MOSFET architectures with a single set of model parameters.

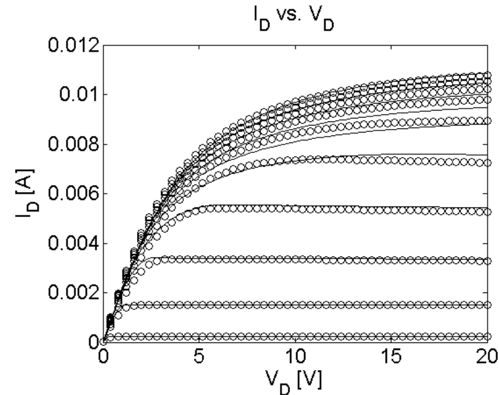

Figure 3. Typical I_d-V_{ds} characteristics of the HV MOSFET

A typical Id-Vd characteristic is shown in Fig.3. The model predicts the quasi saturation of the drain current when the gate voltage is increased, which is indeed a major effect in HV

devices. The same agreement is observed for Id-Vg curves at different drain potential, as shown in Fig.4

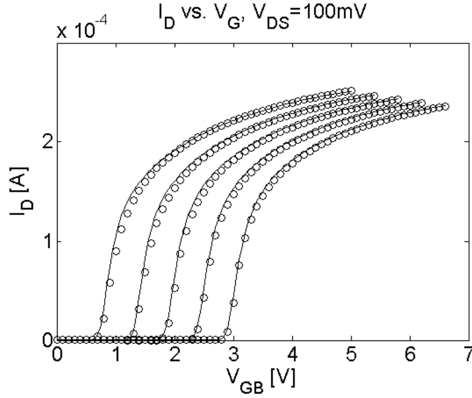

Figure 4. Typical Id-Vgs characteristics of the HV MOSFET

IV. III-V HEMTs

In the last three decades, there have been intense activities focused on the development of reliable non-linear compact models for the simulation of III-V MESFETs and HEMTs [22]-[26]. These models are necessary for the design of modern microwave circuits and systems. Accurate non-linear models are also important for the development of HEMT technology and for the minimization of intermodulation distortion in communication systems. Such models have been continuously improved to study several effects, including temperature effects, frequency dispersion, charge conservation and soft-breakdown [22],[27],[1]. Perhaps one of the most efficient compact models for the study of non-linearities in HEMTs is the Chalmers model introduced by Angelov et al. [28]. This empirical model is capable of accurately modeling the current-voltage characteristics and the associated higher order derivatives, which is necessary for intermodulation distortion studies [30], while simplifying the procedure of model parameter extraction. For medium and high power applications, power dissipation can reach levels causing the heating of the FETs to a given temperature [31]. In the case of III-V HEMTs, such temperature rise may be significant due to the extremely low thermal conductivities of the III-V alloy-based thin layers forming such structures. As a result, there is an increasing demand for reliable electrothermal modeling techniques that account for self-heating in these devices. Several publications have discussed the possibility of considering temperature effects in the framework of the Chalmers model (see for example [22] and [1]), but most of them focused on the effect of ambient device temperature change rather than temperature rise due to self-heating. This work presents a continuous compact DC model for HEMTs (and MESFETs) self-consistently including device self-heating. This involves the extension of the Chalmers model to consider such effects, with a reduced number of fitting parameters while maintaining one of the main advantages of this model: simple model parameter extraction. To demonstrate the continuity of the model, we study intermodulation distortion in submicrometer GaAs pHEMTs using the Volterra series method.

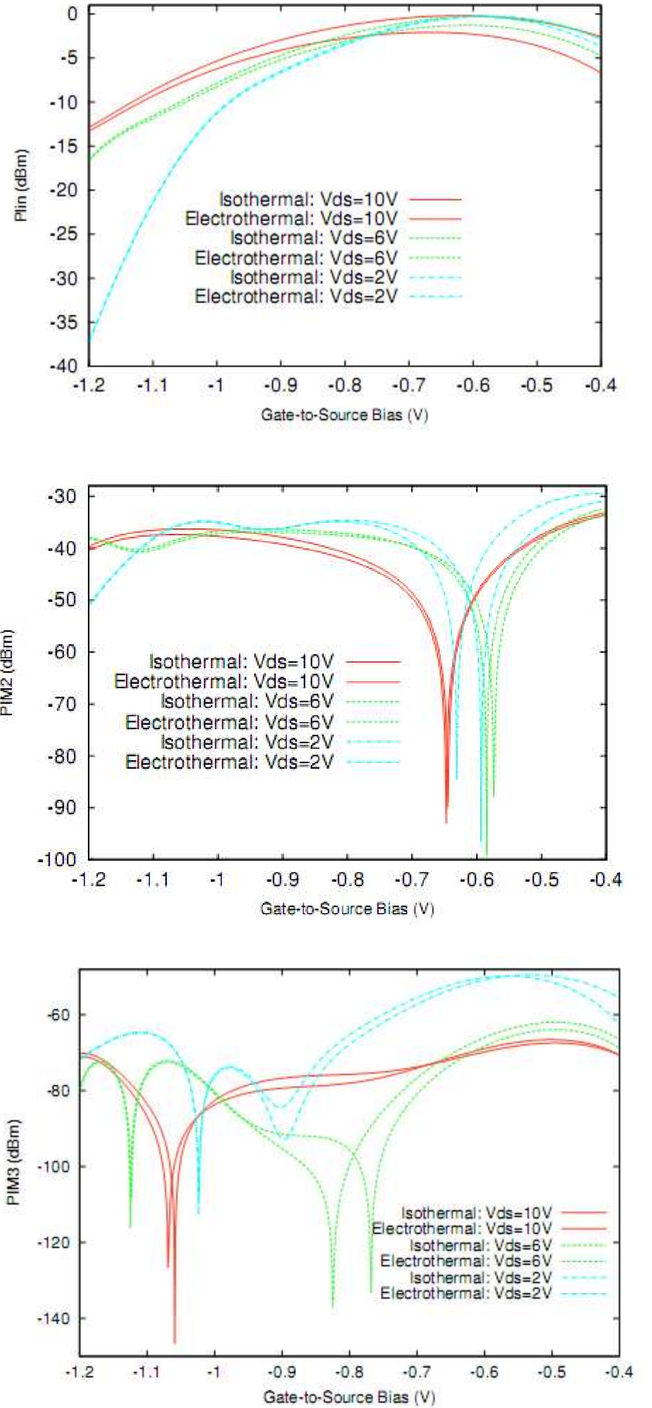

Figure 5. Variation of the linear (P_{lin}), the second- (PIM2) and the third-order (PIM3) intermodulation output power, with V_{gs} for three V_{ds} values.

We apply our model to generate the pulsed (isothermal) and DC characteristics of the 0.25um gate GaAs pHEMT simulated in [34]. This device exhibits significant self-heating, and therefore is ideal to demonstrate the efficiency of our model. Fig. 5 shows the variation of the P_{lin}, PIM2 and PIM3

with V_{GS} for different V_{DS} values. Clearly, the effect of self-heating is more visible on the fundamental linear power P_{lin}, which is reduced at higher drain biases. While isothermal data show higher P_{lin} at higher drain biases, electrothermal data show lower P_{lin} values at higher drain biases, at gate biases higher than 0.7V where the influence of self-heating is significant. The model, which is based on the standard Chalmers model, uses simple analytical expressions to accurately account for self-heating, while minimizing the need for parameter fitting and allowing simple model parameter extraction. The continuous nature of this model makes it suitable for intermodulation distortion, as demonstrated using the Volterra series method.

V. STATISTICAL MODELING APPROACHES

Scaling and increasing complexity of a CMOS technology leads to an increasing influence of the MOS transistor parameter and characteristics variability for the CMOS integrated circuit (IC) performance. This variability results from a granularity of a matter in materials used for IC fabrication, from a spread of CMOS IC fabrication conditions, and from the not-fully controlled phenomena (e.g. stress) [36],[37]. The spread of parameters/characteristics leads to manufacturing yield degradation. In spite of the efforts towards minimization of parameter spread (strict following of the manufacturing recipes, use of undoped or lightly doped SOI substrates) it is unavoidable, thus must be taken into account at the design phase.

A. *Statistical modeling Approaches*

There are two main approaches used for global variation modeling in the IC design process: corner analysis (CA) and Monte-Carlo (MC) simulation methods. The CA method enables evaluation of the circuit performances, resulting from the extreme values expected in the process, supply bias and temperature (the corners) [38]. It requires simulation in each corner defined by the set of requirements. Typically, these requirements imply maximization or minimization of saturation current at maximum applied voltages by setting the model parameters to their upper and lower values. In the case of a simple set of performance measures (in the case of digital CMOS ICs) the number of corners and the number of simulations is small. However along with the increasing number of performances taken into account (e.g. CMOS analog blocks) the number of corners and simulations significantly increase. Moreover, in general the CA method gives a very pessimistic estimation of the circuit performances, because it ignores the existing correlation between model parameters. The MC method consists in calculation of the circuit performance distributions resulting from statistical distributions of model/device parameters. The method takes advantage of the compact model structure. Usually there is a subset of model parameters (**m**) which can be considered as preferably non-correlated process parameters (**p**), which may be varied independently. The method is dedicated for physical models with a small number of fitting parameters. A simplified flow-chart of the MC method is shown in Fig.7. The MC method allows specifying much more precisely a safe area of the IC design than the CA approach.

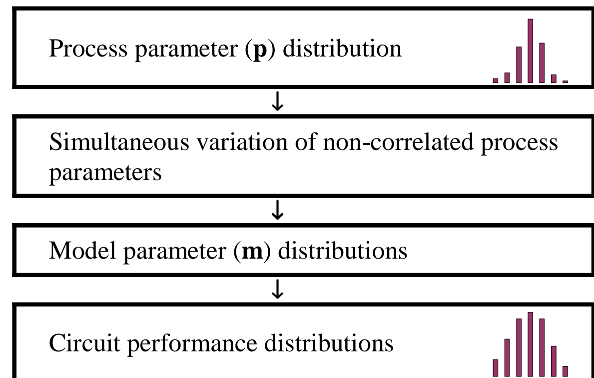

Figure 6. Flow-chart of typical Monte-Carlo simulation.

In order to accomplish the task of the IC design including the statistical variability the simulation tool must be supplied with information about distribution of model parameters responsible for IC performance variability. Derivation of variability of circuit performances (standard deviations or variances) for a given, stable, and characterized process, and for a given device model is the main task of a statistical modeling.

B. *Statistical modeling methods*

Statistical modeling is based on analysis of large amounts of experimental data in the form of I-V, C-V characteristics, or functional tests of the dedicated test circuits. The collected data are subject to statistical analysis, and used for evaluation of statistic distributions of model parameters (preferably uncorrelated) responsible for IC performance variability. There are several methods used for this purpose, e.g. the principal component analysis (PCA), forward propagation of variance (FPV), and backward propagation of variance (BPV). Based on the PCA method (e.g. [39]) a set of uncorrelated formal (physically meaningless) random variables is determined, which the model parameters are correlated with. These variables serve as generator of model parameter distributions used for the MC analysis purpose. The FPV method (e.g. [40]) allows determining directly distributions of selected model parameters. However this method may lead to correlated parameter distributions, which can not be used in MC analysis. The disadvantages of the PCA and FPV methods may be overcome using the BPV method (e.g. [41]). It is an efficient method for analysis of the correlated data and, based on this, for estimation of the variances of uncorrelated parameters describing the manufacturing spread and responsible for device characteristics variability. The general idea of the BPV method is illustrated in Fig.6.

The method starts from the electrical measurements of the so-called process control monitors (PCMs), which are test structures consisting usually of transistors of different geometries, and of simple digital or analog blocks. The

electrical tests give measurement data **e**. Next the variances of **e** data are expressed as linear combinations of process parameter **p** variances. For the given model this leads to over determined (usually) set of linear equations against variances (σ_p^2). For the purpose of further considerations the EKV model [42] has been used. The process parameter set **p** may consist of

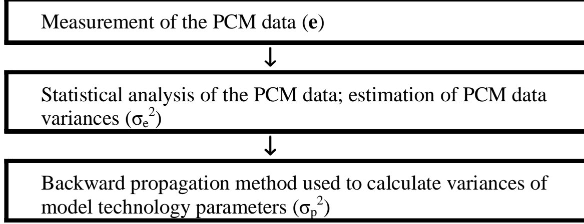

Figure 7. Flow-chart of the BPV method.

the following parameters: TOX, log(NSUB(N)), UO(N), DL(N), DW(N), log(NSUB(P)), UO(P), DL(P), DW(P). Indices (N), (P) denote parameters for n- and p-channel devices. It is worthwhile to mention, that gate oxide thickness has been selected as random variable common for both device types. In this case the mentioned above set of linear equations against variances σ_p^2 may be written in form (1). The sensitivity matrix S below is calculated from SPICE simulations using finite difference method.

$$\begin{bmatrix} \sigma^2_{Vth(P)} \\ \sigma^2_{Idsat(P)} \\ \sigma^2_{gm(P)} \\ \sigma^2_{rds(P)} \\ \cdots \\ \sigma^2_{Vth(N)} \\ \sigma^2_{Idsat(N)} \\ \sigma^2_{gm(N)} \\ \sigma^2_{rds(P)} \\ \cdots \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & \cdots \\ S_{21} & S_{22} & \cdots \\ \cdots & \cdots & \ddots \end{bmatrix} \begin{bmatrix} \sigma^2_{TOX} \\ \sigma^2_{\ln NSUB(P)} \\ \sigma^2_{UO(P)} \\ \sigma^2_{DL(P)} \\ \sigma^2_{DW(P)} \\ \sigma^2_{\ln NSUB(N)} \\ \cdots \end{bmatrix} \qquad (1)$$

$$\boldsymbol{\sigma}_e^2 = \mathbf{S}\,\boldsymbol{\sigma}_p^2 \;;\quad S_{ij} = \left(\frac{\partial e_i}{\partial p_j}\right)^2$$

A very important issue is specification of the PCM performances, used for extraction of **p** set elements standard deviations, and for calculations of the sensitivity matrix **S**. The performance set should cover the whole range of device geometries, of supply bias, and as wide as possible range of operation conditions. Furthermore,, they should respond to variations of the mentioned above manufacturing conditions, temperature, and bias. In a current status of our research, and taking into account availability of test structure measurement data we have selected the PCM data listed in Table I.

TABLE I. PROCESS CONTROL MONITOR PERFORMANCES LIST

Device	*Name*	*Description*
Large	V_{th}	Lin. V_{th} at low V_{ds} for large device
	Idsat	Sat. drain current for large device
Short	g_m	Peak transconductance
	V_{th}	Lin. V_{th} at low V_{ds} for short device
	I_{dsat}	Sat. drain current for short device
Narrow	V_{th}	Lin. V_{th} at low V_{ds} for narrow device
	R_{ds}	Out. resistance at max. biases
Small	V_{th}	Lin. V_{th} at low V_{ds} for small device
	Idsat	Sat. drain current for small device

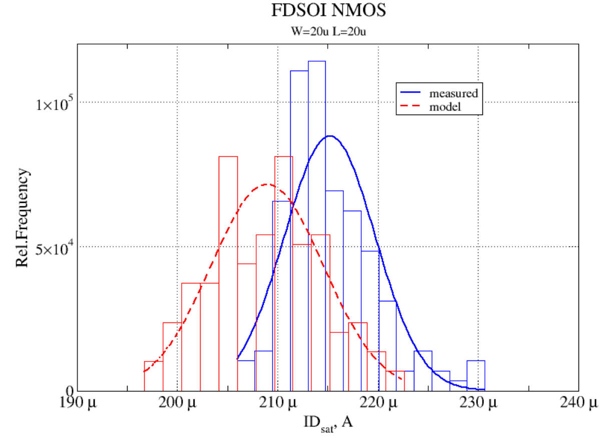

Figure 8. Histograms of the saturation current (I_{Dsat}) of FD SOI NMOSFETs (W=20 µm, L=20 µm) measured and simulated using process parameter variances determined based on the BPV method.

C. Implementation

The BPV approach has been examined within COMON project. At the first stage the trial pseudo-measurements of the PCMs have been generated using the SPECTRE program. For this purpose the predefined Gaussian distributions of the selected process parameters have been assumed. Using the proposed methodology the variances of these parameters have been reproduced. The agreement between initial and final variance values has been satisfactory. The differences between them have been not more than 5% [43]. In the next phase the methodology has been tested against the real measurement data obtained for series of devices manufactured in ITE using the FD SOI CMOS technology acquired from UCL within FP7 project TRIADE [44]. In Fig.7 there are histograms of I_{Dsat} current of FD SOI NMOSFETs (W=20 µm, L=20 µm) measured and simulated using process parameter variances determined based on the BPV method. The agreement is not satisfactory, however it should be mentioned, that the technology is in the phase of implementation, so for sure it can not be considered as a mature, stable one.

VI. COMPACT MODEL VERILOG-A STANDARDIZATION

The achievement of this goal depends on the adoption of Verilog-A by all the actors concerned: final users, semiconductor foundries, compact model developers as well as EDA vendors. But both final users and semiconductor

foundries cannot accept degradation in simulation speed or loss of functionality. This paper introduces the sub-set of Verilog-A needed to write efficient compact models for different Verilog-A simulators. And, as SPICE simulators remain faster than most Verilog-A simulators, this paper presents some guidelines to help compact model developers improve the integration of their Verilog-A models into SPICE simulators while reaching the speed and the functionality of C code based compact models [47].

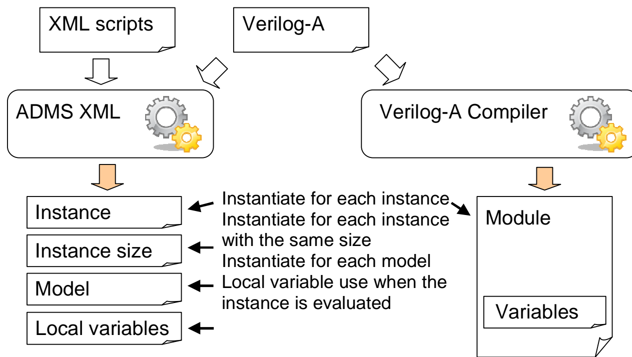

Figure 9. Memory decomposition in SPICE versus Verilog-A

With the SPICE compatibility extensions of the Verilog-AMS Language Reference Manual (LRM) version 2.3.1, Verilog-A [46] has the potential to revolutionize the paradigm of analog design of integrated circuits and totally replace SPICE.

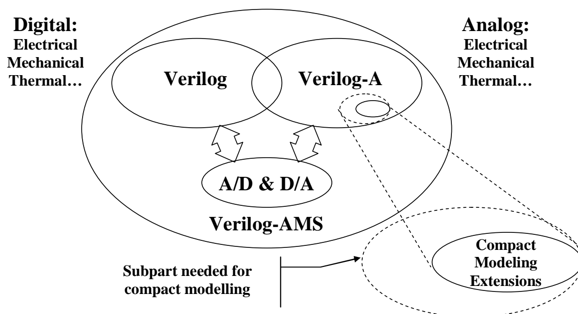

Figure 10. Compact Modeling Verilog-A subset

A recent study [48]-[49] shows that under some conditions, some Verilog-A simulators can be as efficient as SPICE simulators. The ball is now in the camp of the standard groups and EDA vendors to make Verilog-A simulators as fast as their SPICE counterparts, as well as to allow Verilog-A to address the challenges of deep submicron processes such as process dispersion, dynamic degradation, power consumption, system-level complexity.

TABLE II. CPU TRANSIENT TIME RESULTS

Simulation time (seconds)		SMASH 5.15		Simulator B		Ratio Verilog-A / SPICE
		SPICE	Verilog-A	SPICE	Verilog-A	
PSP Model	Circuit #1	**1.1s**	**17.7s**	2.61s	30.1s	16.1
	Circuit #2	**17.2s**	**249.7s**	29.95s	416.8s	14.5
	Circuit #3	**206.9s**	**3384s**	284.6s	8 822s	16.4
EKV3 Model	Circuit #1	**2.43s**	39.7s	NA	**31.8s**	13.1
	Circuit #2	**31.3s**	594.9s	NA	**351.8s**	11.2
	Circuit #3	**372.7s**	Too Big	NA	**10 197s**	27.4

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