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FOR IMMEDIATE RELEASE

PLATINUM SIMULATOR SMASH 4.4 LAUNCHES DYNAMIC ELECTRICAL RULES CHECKING (ERC)

DOLPHIN Integration and ELMOS Semiconductor celebrate eight-year partnership with scores of IC Simulation Stations

Grenoble, France, December 6th, 2001 – At the opening of the "IP based Design" conference, DOLPHIN Integration of Meylan, Dauphiné, France and ELMOS Semiconductor AG of Dortmund, Germany, are announcing a breakthrough in quality, reliability and yield for mixed signal IC design.

The platinum paradigm

A small number of traditional analog simulators are treated as so-called Golden Standard for process qualification, while innovative mixed signal simulators like SMASH may serve both as standard and as productivity enhancing, so-called Platinum standard for new process and product certification, enabling debug, calibration and yield improvement.

Such a focus on improving quality, reliability and yield through better simulation aims at providing SoC designers with the most appropriate, accurate and robust simulation solution. DOLPHIN Integration and ELMOS thus cooperated for ensuring that such a label would correspond to pragmatic and drastic improvements for the designer.

This partnership ensured that the joint focus was away from bridling innovation by standardization, but instead on true concerns for user's productivity improvement.

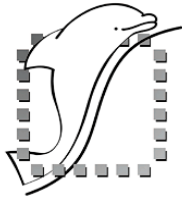
Emphasis was thus turned to the development of dynamic ERC firstly to flag checks of Safe Operating Area (SOA) for high voltage sub-micron CMOS for overshoot of supply voltage on transistors, for tracing, pause and restart.

Dynamic Electrical rules Checking

There is an increasing importance for designers to be able to perform ERC and SOA checks in order to control that circuits variables (current, voltages, powers, threshold and saturation voltages, internal variables, etc.) stay inside a given interval or do not exceed predefined limits (maximum or minimum).

"High Voltage Sub-Micron CMOS in combination with analog / mixed-signal design is a tough challenge, dear to the automotive industry, and ELMOS strives to maintain its leadership" boasted Ludger Krücke, V.P. of Engineering.

These electrical design rule checks are an important aspect in obtaining design compliance with the specifications and guaranteeing safe operation. The aim is to catch mistakes early in the design process and the rules enforce a consistent design methodology. Above all, dynamic ERC significantly increase productivity in netlist finalization.



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Implemented in SMASH, it will allow the simulation to be paused, aborted when a rule is violated in order for the designer to be able to analyze and debug the circuit.

"We are quite thankful to ELMOS for partnering with us, a company at the cross-roads of reliability and cost concerns, for whom yield is so essential, that they dare look for the best design enabling technologies, beyond the prevalent CAD frameworks" stated Gilles Depeyrot, Development manager for Dolphin's EDA.

The partners' objective is most encompassing and aims at providing the required functionality within our larger offering. The implementation of electrical rule checking will be the basis for future developments on analog mixed-signal circuit debug.

A long-term partnership

The initial impetus for this endeavor was the shared belief that design flows had to be freed from any monopolistic practice related to Frameworks, Machines Operating Systems, as well as design language standards. In the early nineties, the first improvements came with identical availability on UNIX and Windows - and now Linux - of the SMASH simulator and diverse Schematics Entry packages.

This cooperation went further when ELMOS invited DOLPHIN in the European project ROBAS - for Robust ASIC design flow - to enable the first full implementation of the VHDL language in the celebrated mixed language simulator, thus bringing this language at par with VERILOG-HDL.

The striking consequence is the prevalence today of VHDL-AMS over any other mixed signal language, and its most effective implementation in SMASH.

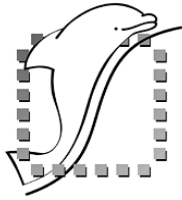
A multilingual world

Today, SMASH is the only genuine mixed signal, multi-level simulator on the market. Mixed signal means that SMASH handles both analog, continuous signals, and discrete digital signals. Multi-level means that SMASH is by no way limited to the circuit or structural level - it also handles functional and behavioral levels, for both analog and digital worlds. Thanks to this bi-dimensional flexibility, you can use SMASH for virtually any kind of design.

For maximum compatibility with other EDA tools, SMASH uses SPICE syntax for analog descriptions, Verilog-HDL and VHDL for digital, VHDL-AMS and ABCD (a combination of SPICE and C) for analog behavioral, and C for DSP algorithms.

VT&D plus patented yield improvement

Modeling, simulation and Virtual test can no longer be loosely confused: a Platinum simulator must provide a full array of capabilities in all three dimensions. Modeling must be either open (i.e. revealing the design specifics like SPICE) or "black-box" like VHDL-AMS describing pure behavior. Simulation must be all-encompassing, to the point of enabling physically unrealistic conditions. VT&D on the contrary must enable physically realizable conditions on an open-box, relying on an array of Testbench description languages like



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VHDL-AMS, C... up to emulator features with the generalization of "Trace and Stop on Event". The improvement of productivity in simulation analysis is impressive. To be the real leader in the Verification World, SMASH thus innovates in debug, calibration and yield improvement.

Patent as proof of innovation

When you consider a circuit requiring similar MOS transistors, even if their layouts are strictly identical, behaviors may differ because of fabrication randomness. Engineers use Monte Carlo analysis to checking whether their design is secure enough. Random dispersions related to transistor matching, capacitance uncertainty... systematically degrade the expected characteristics and yield of analog circuits. To predict properly the analog characteristics and yield of such circuits, it is necessary to take into account crucial random dispersions in the simulation process to select the optimal circuitry.

DOLPHIN has introduced in SMASH a new technique, which allows meticulous verification but also the possibility to diagnose the transistors sensitive to such matching effects. A pending patent shall demonstrate this state-of-the-art technique enabling yield loss prediction for every design critical issue: device matching, noise, current peaks... Moreover, when performed at the first stages of simulation, an earlier diagnostic of potential yield losses enables an important improvement of productivity and Time-To-Market (TTM).

The method is based on the use of Monte Carlo simulations within an optimization loop including the simulation engine and the circuit model. It ensures the possibility to reproduce any draw of a set of Monte Carlo simulations in order to optimize design performances in the presence of sensitivities to random dispersions.

This paves the way to a next generation of "Electrical Stress Checking" which would take into account "metal stress relief rules", etc. beyond the classical "electrical design rules" found in most "Design Rules Manual". The era when Verification was a static issue involving only DRC and LVS is over, and simulation has become essential for dynamic verification.

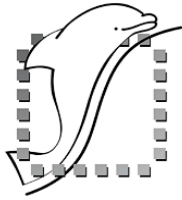
Simulated for Right-on-first pass

Up to 70% of the project development costs of a System on Chip are allocated to verification by simulation, a gain of productivity, thanks to tools with result analysis of the simulation results, speed up TTM, and reduce development costs.

Providing the traditional IC design flow with some credible new paradigm for TTM is not achievable through the mere upgrades: the partners are proceeding through a real disruption with this breakthroughs providing both IC Makers and System designers with capability for safe and swift delivery.

ELMOS is now well ahead with expertise in integrated circuits design for automotive applications, well-known for wanting space or military quality at consumer prices.

Both ELMOS and DOLPHIN Integration want to make their respective competencies in IC's and Silicon IP better known to the semiconductor community, with such a blockbusting improvement for their customers.



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About DOLPHIN Integration

This European Enterprise, provider of "Service Empowered IP" for Logic, Analog and Memory Virtual Components, offers the FLIP™ "Flexible Line of Integration Platforms" with design services and support. Its German subsidiary specializes on MEMS. They operate jointly from turnkey design to consulting support for customers wanting efficient insertion of FLIP cores from kits into their SoC design. Dolphin is a member of the Virtual Socket Interface Alliance (VSIA) and of the Virtual Component exchange (VCX).

The corporate charter is to help customers meet the challenges of time-to-market with a quality control process leading reliably to success on first pass. For additional information you can find Dolphin at www.dolphin-ip.com or address your inquiries to medal@dolphin-integration.com.

About ELMOS Semiconductor

ELMOS is one of the market leaders for customer and application specific integrated circuits (ASICs) especially for the automotive industry. Based on more than fifteen years of experience and hundreds of different products, ELMOS can offer you dedicated analogue / mixed-signal system-on-chip solutions for smart-power applications.

With the customizing business model, ELMOS supports its customers to protect their know-how, assists them to improve the quality and the reliability of their system and helps them to reduce their system costs. More than hundred engineers in Germany, France and the U.S.A. are involved in the research and development of dedicated process technologies, design-libraries and of course new products.

Design, development and production at ELMOS are certified according to the most stringent international quality standards including ISO 9001, QS 9000 and VDA 6.1.

For more information you can visit ELMOS at www.elmos.de or sent your requests to info@elmos.de.

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